

NMIS/L-7041
4-Channel Low Power
Bipolar Stepper Motor Driver Card



GETTING STARTED

The NMIS-7041 Low Power Bipolar Stepper Motor Driver Card provides a JEDSTACK™ computer system with four channels of low power stepper motor drive. Each of the four On Semiconductor MC3479 Low Current Stepper Motor Driver Chip provides circuits (bipolar transistor technology) for driving a two-phase stepper motor in bipolar mode. The chips consist of four input sections, a logic decoding/sequencing section two driver-stages for the motor coils and an output to indicate the Phase A drive state counter and a code converter to drive the four outputs in the required sequence. The step and direction control lines are placed in the memory mapped by the interfacing logic on the card. A register with individual bits representing these lines allows processor control of the stepping occurrences and direction of rotation.

To make use of the NMIS-7041 requires physical installation, addition of the necessary software. The remainder of this section deals with these steps in greater detail. The user will probably want to read this section once, then scan the Circuit Description, Register and Programming chapters before taking any action, then again return to this section and follow the suggested installation procedure. Finally, the other sections will tell more on the board's design, mechanical board mounting and problem solving troubleshooting approaches.

A few moments spent examining the NMIS-7041 will be useful. The 2x4 inch format of the NMIS board series determines the physical outline of this board. Close observation of the board reveals the following features. The four Stepper Motor Driver chips, On Semiconductor MC3479, are the key parts on the board. Each is located next to its motor connector in the upper left hand corner of the board (top view). The motor connectors are 10 pin dual .1" center male pins. This On the outer row, the five pins are connected to +V. On the inner row, four pins are connected to the four phase outputs and one pin is the return for the current programming resistor. Next to each MC3479 is a pair consisting of a resistor and capacitor. This RC pair decouples the noisy +V signal from the logic sections of the chip. The 74HC574 and 74HC245 comprise this computer readable-writeable latch. A Vertical Stacking Connector in the lower right hand corner provides connections to the processor's address and data bus, control signals, 5 Volt power and ground. Two octal comparators, 74HC688's, and 16 two-position jumpers, accomplish address decoding in memory. Each jumper setting corresponds to the state of a particular address line. The NMIS-7041 occupies one address. Any single byte location in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement. The 74HC139 further qualifies the address selection with the timing and direction signals from the bus to generate the strobes to the latching chips.

To install the NMIS-7041, the following procedure is suggested:

1. Select the address (or accept the factory default)
2. Set the jumpers for the selected address (or check the factory default)
3. Verify the selected address is free of memory conflict before installing the board
4. Turn off the power to the system
5. Install the board connecting the VSC
6. Verify correct alignment visually
7. Turn on system power
8. Verify the presence of the board in memory
9. Turn off the power to the system
10. Select the motors to be used
11. Connect the motors to be used
12. Select the current programming resistor
13. Connect the current programming resistor
14. Connect motor drive power
15. Turn on system power and motor drive power
16. Select the program or program segments to be used
17. Install the program or program segments to be used

Selection of the address for the board will depend greatly on the processor card being used, system design, and how many other boards are being used in the system. For instance, the most popular CPU to date that can use the NMIS-7041 is the F68HC11 based NMIS-L-0021B. Although there could probably be valid reasons for mapping the RTC almost anywhere in the 64K byte address space, a likely place would be in the B000 hex area above the registers. If no additional 2x4"STM cards were in the system, B040 hex is a likely choice. On the other hand, an address above the EEPROM at BC00 hex would have more merit for both the NMIS-0021 CPU and the NMIX-0022 alike. The NMIX-0022 CPU's have a 68HC24 PRU that is loosely decoded in the B000 through B7FF hex range. Putting the RTC at BC00 would clear any possible memory conflicts there, while having minimal impact on the greater goal of leaving large areas of contiguous memory unbroken. The older NMIX-0011 and NMIX-0012 CPU's can use the NMIS-7041, but these boards use the 0100 hex page for I/O. In this case an address such as 0110 hex would be appropriate.

Once an address is selected, it is easy to set the jumpers. Convert the address to a binary number and, starting left to right, set the jumper corresponding to each bit in the binary number to a "1" or "0". Refer to Appendix A for graphic examples. The factory default address setting for the NMIS-7041 is 8000 hex and will be used in these examples. Substitute the corrected value in place of 8000 hex if the base address has been modified. It is advisable to verify the selected address is free of memory conflicts before installing the board. First look at the memory addresses the RTC will occupy to see if other devices are already mapped there. These could cause interfere, called, bus contention. Dumping the area around 8000 will normally show an ascending number pattern if no memory interferes, as is shown below in a dump by an F68HC11.

```
COLD
Max-FORTH V3.5
HEX OK
8000 40 DUMP
8000 0 1 2 3 4 5 6 7 8 9 A B C D E F
8010 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
8020 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F
8030 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F
OK
```

Selection of the correct motor for a job depends on many variables. Beyond supply issues, motors are qualified by step angle (also labeled as steps per revolution), maximum torque, maximum revolutions per minute (or second), maximum pull-in rate in steps per second, etc.. For the purposes of this document the voltage and current rating limitations of the driver chips will be the primary limitation on motor selection. The MC3479 chips are capable of driving motors with 500mA per stator (350mA nominal) from a 9.5 to 18 Volt supply (12V nominal). Since the drivers can accommodate motors of differing current ratings, a method of selecting the drive level for each motor is provided. The desired current is selected by adding a programming resistor to the motor connector, R1-4. The value of the resistor with the power off to the system, carefully align the 34 pin Vertical Stacking Connector (VSC) with the board to be mated. The VSC is a "straight through" connector so the NMIS-7041 can be added to the top or the bottom of a board stack. It's easy to get a misalignment, so double check the fit by looking at the connector from all four directions for pins that are not correctly mated. Use the provided 4-40 male/female screw 3/4" brass hex standoffs in the hole adjacent to the VSC to increase mechanical rigidity. Turn the system power on write a known value to the board location and examine the memory area around 8000 hex again.

```
COLD
Max-FORTH V3.5
HEX OK
FF 8000 C!
8000 40 DUMP
8000 FF 1 2 3 4 5 6 7 8 9 A B C D E F
8010 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
8020 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F
8030 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F
OK
```

Notice the first location now has a different value. This is the register that allows manipulation of the control lines of the MC3479 Low Current Stepper Motor Driver chip. Its contents will, of course, vary depending on the power up setting taken by the latches. In order to recognize the register in memory a known value is first written to it. If the ascending pattern has not changed, the processor can not "see" the NMIS-7041 in its memory map. Recheck the address jumpers for proper settings and the VSC for proper

connection. The Programming Chapter and Appendix B have selected program segments, which can be used to read and write the Stepper Motor control register. Writing proper programs requires a detailed understanding of the functions of the MC3479's and the bit positions associated with each control line. To begin with, copying the programs from those sources may be expedient. Install the program or program segments to be used. The NMIS-7041 is now running and communicating, as it should.

CIRCUIT DESCRIPTION

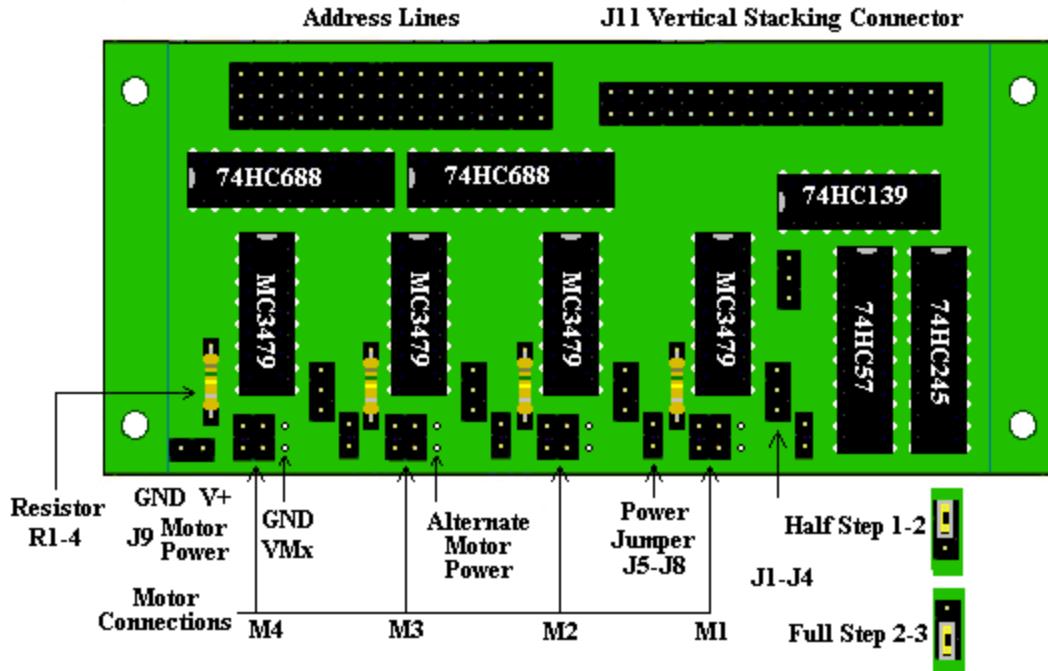
The NMIS-7041 Stepper Motor Driver card is designed to stack on the 2"x4"s™ NMIS Series, or 2"x4.75" NMIL-Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The JEDSTACK™ provides the interface signals to the board including address lines, data lines, control lines and 5 Volt power and ground. The fast HC latches allows 90nS access times.

The addressing of the 74HC574 (U8) and 74HC245 (U9) register pair on the NMIS-7041 is sensed by two 74HC688 (U5 and U6) octal comparators that decode the 16 address lines (A15 - A0) and one control line (AS for F68HC11 systems, CSEX for R65F11 systems) to select only one active location out of a 64K address space.

The address location where the card is active is user set by the arrangement of addressing jumpers. Each address line can be sensed for high or low condition. (Jumpers were used rather than switches for power savings reasons. Generally schemes that employ switches use pull up resistors that are switched to ground for a "0" and left open for a "1". When the switches are closed this means the resistors are hooked from the +5V rail to ground. While this gives the comparator inputs a suitable logic level "1" or "0", the selection of "0" wastes power. The design using jumpers hook the CMOS comparator inputs directly to +5V or Ground without wasting power.)

When the processor selects one of the sixteen set addresses, the 74HC688's generate a chip select to the 74HC139 (U7). This signal is also coupled back on the VSC via diode D4 to the MEMDIS pin. The 74HC139 further decodes the generated chip selects to provide a separate read strobe for the 74HC245 and write strobe for the 74HC574. Gating the chip select with the processor's Output Enable signal generates the read strobe. Gating the chip select with the processor's Write signal generates the write strobe. The output of jumper J10 is also used to gate the write strobe. In cases where the processor does not have timing impressed on the Write signal, J10 should be set to pass the "65" for HC11, or set to "80" for 8051 controller interface for clock timing signal to the decoder. The 74HC574 accepts data from the processor, over the parallel Data Bus, when the read strobe is active. This latched data is applied to the 74HC245 for read back. The 74HC245 sends data to the processor, over the parallel Data Bus, when write strobe is active.

The four Stepper Motor Driver chips, On Semiconductor MC3479, are the key parts on the board. Each is located next to its motor connector in the upper left hand corner of the board (top view). Detail technical data sheet can be downloaded from, <http://www.onsemi.com/pub/Collateral/MC3479-D.PDF>



The motor connectors, M1-4 are 4 pin dual .1" center male pins. On the right hand side of each motor connector, there are 2 pin labels VMx & GND. These pins are dedicated for motor power connections when multiple motor power sources are required for different type of motor. In this case, J5-8 jumpers need to be removed.

Next to each MC3479 is a 150K socketted resistor, R1-4. These are the motor limiting current resistor, and they are removable to allow user to select the appropriate resistor value to meet there motor spec and requirements. R1-4 can be calculated as below,

$$R_b = (V_m - 0.7) / I_{BS}$$

For example, assume an application where $V_m = 12$ V, the motor requires 200 mA/coil, operating at room temperature with no heatsink on the IC. IBS is calculated:

$$I_{BS} = 200 \times 0.86$$

$$I_{BS} = 172 \mu A$$

RB is calculated:

$$R_B = (12 - 0.7) V / 172 \mu A$$

$$R_B = 65.7 k$$

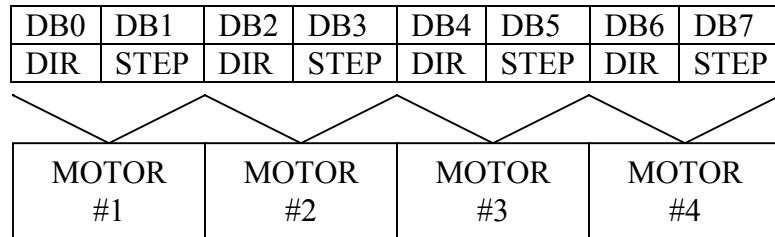
More details explained on page 8 and 9 of the MC3479 data sheet.

<http://www.onsemi.com/pub/Collateral/MC3479-D.PDF>

The 74HC574 and 74HC245 comprise this computer readable-writeable latch. A Vertical Stacking Connector in the upper right hand corner provides connections to the processor's address and data bus, control signals, 5 Volt power and ground. Two octal comparators, 74HC688's, and 16 two-position jumpers accomplish address decoding in memory. Each jumper setting corresponds to the state of a particular address line. The NMIS-7041 occupies one address. Any single byte location in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement. The 74HC139 further qualifies the address selection with the timing and direction signals from the bus to generate the strobes to the latching chips.

REGISTERS

The processor has access to the MC3479 control lines through the on board register of the NMIS-7041. The processor can control the state of two lines on each MC3479.



DIR: direction

STEP: Pulse

PROGRAMMING

Writing drivers for the NMIS-7041 is relatively easy. (A set of software drivers is included in the PROGRAM SEGMENTS appendix.) The control register is read or written in a straightforward manner.

BOARD MOUNTING

The NMIS-7041 has three mounting holes, one in the corner nearest the 34 pin Vertical Stacking Connector which is the main mechanical mounting hole, and two in the opposite corners used for alignment. Each hole is drilled at .110 inches. This will allow passage of a 4-40 screw shaft.

If additional 2x4"sTM are to be used they may be stacked above or below, as desired, on the female or male side of the Vertical Stacking Connector respectively. A simple hex 3/4-inch standoff with a male screw on one end and a female threaded hole on the other is the ideal inter board connection device. The Vertical Stacking Connector was designed to work with this size spacer, giving reliable board-to-board connection.

The length of the standard spacer, 0.750 inches, plus the board thickness, 0.061 inches, gives a nominal spacing board to board of 0.811 inches. If an exact spacing of .800 inches is desired (some standard mounting hardware have .800 inch mounting board guides) 0.011 inches of the mounting surface at the female end of the soft brass standoff can be removed by mill or metal file.

Only the mounting hole near the Vertical Stacking Connector has sufficient clearance around the hole to allow for the head of a screw or the flats of the standoff to rest on. The trace closest to the hole is GND on the topside of the board. All 2x4"sTM are designed with this same convention.

The two mounting holes at the other end board can be used for alignment pins, but do not have sufficient clearance to allow the use of screw. All 2x4"sTM attempt to follow the convention, maintaining these two mounting holes. If, however, there is sufficient reason to use that board space they may not always be preserved.

The extremely small size of the boards means there is no guaranteed limits on how close components will be placed to the edge of the 2x4"sTM. Board guides will be difficult to use and designs should take this into account. They may be acceptable if non-conductive and very shallow. The main mounting hole remains the best point of support.

TROUBLESHOOTING

The NMIS-7041 is a fairly simple and straightforward board. The most likely problem encountered remains "operator error". There are a minimal number of things that could be wrong otherwise.

JUMPERS

ADDRESSES 8000 HEX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
															
															

ADDRESSES 011F HEX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
█	█	█	█	█	█	█		█	█	█					

ADDRESSES BC00 HEX

PROGRAM SEGMENTS

COLD
HEX
400 DP !

8000 CONSTANT STEP-REG

VARIABLE DELAY-VALUE 100 DELAY-VALUE !
VARIABLE LEFT-SWING C8 LEFT-SWING !
VARIABLE RIGHT-SWING C8 RIGHT-SWING !
VARIABLE ACTIVE 2 ACTIVE !

: L STEP-REG C@ . ;

CREATE PATTERN-TABLE

00 C, (0)
01 C, (1)
04 C, (2)
10 C, (3)
40 C, (4)

: MOTOR-SELECT (1,2,3,4) 1 MAX 4 MIN PATTERN-TABLE + C@ ACTIVE ! ;

: LEFT STEP-REG C@ ACTIVE @ OR STEP-REG C! ;

: RIGHT STEP-REG C@ ACTIVE @ FF XOR AND STEP-REG C! ;

: TOGGLE STEP-REG C@ ACTIVE @ 2* XOR STEP-REG C! ;

: WAIT DELAY-VALUE @ 0 DO LOOP ;

: STEP TOGGLE WAIT TOGGLE WAIT ;

: RUN 0 DO ?TERMINAL IF LEAVE THEN STEP LOOP ;

: SEARCH

 BEGIN
 RIGHT RIGHT-SWING @ RUN
 LEFT LEFT-SWING @ RUN
 ?TERMINAL
 UNTIL

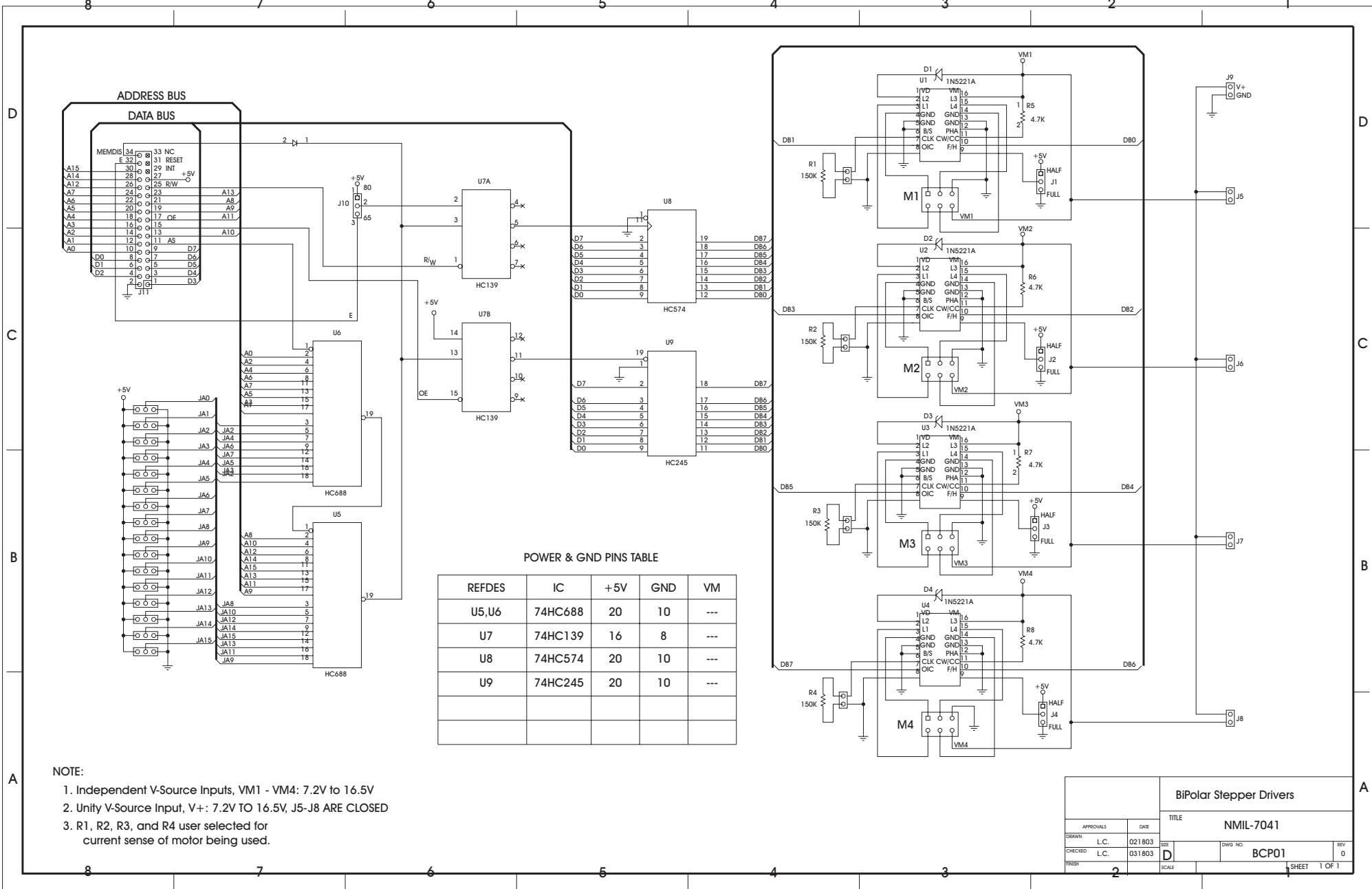
;

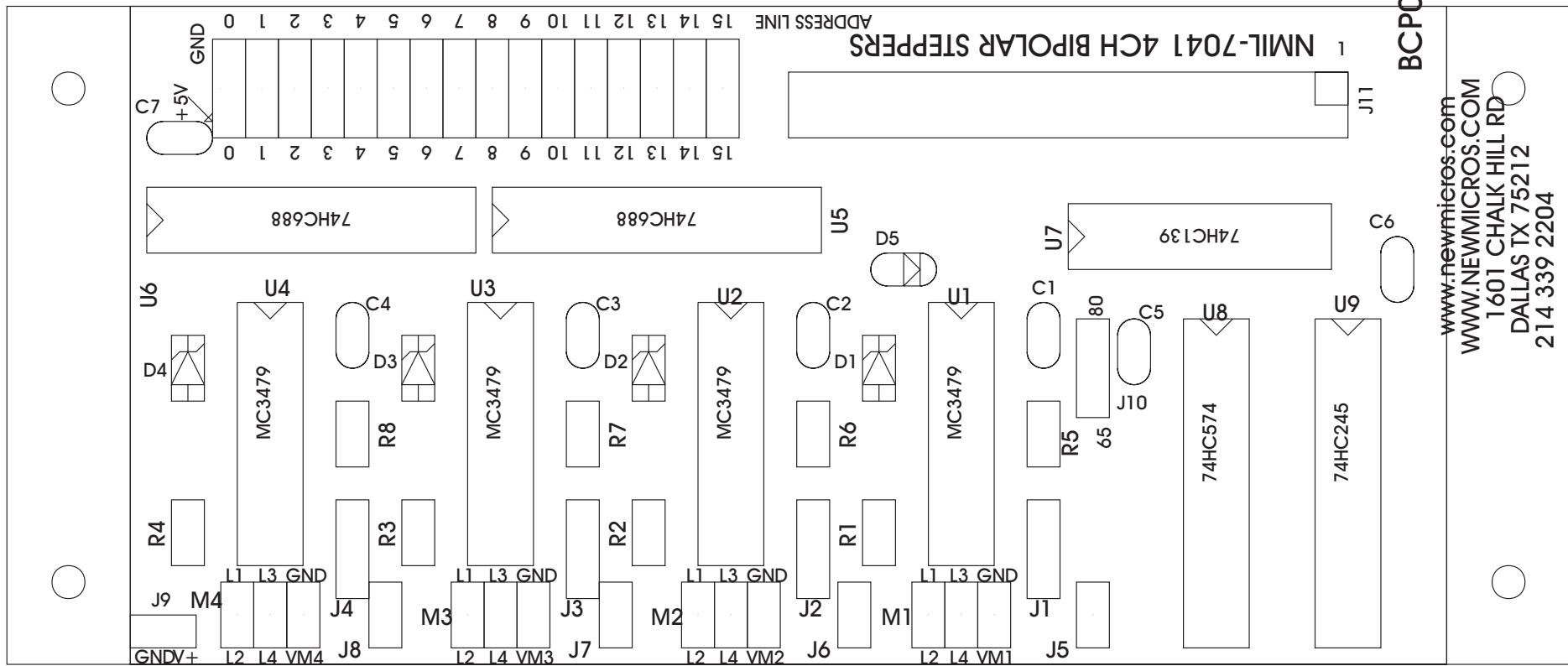
PARTS LIST

NMIS-7041 Low Current Stepper Motor Driver PARTS LIST REV 1.0

PART#	GENERIC	DESCRIPTION
U5,6	20 PIN SOCKET 74HC688	OCTAL COMPARATOR
U7	14 PIN SOCKET 74HC139	DUAL 2-TO-4 DECODER
U1-4	16 PIN SOCKET MC3479	Low Current Stepper Motor DRIVER
U8	20 PIN SOCKET 74HC574	OCTAL LATCH
U9	20 PIN SOCKET 74HC245	OCTAL DRIVER
J1-4,10	3 PIN HEADER	BERG STYLE .1" CENTER JUMPERS
J5-9	2 PIN HEADER	BERG STYLE .1" CENTER JUMPERS
J11	34 PIN VSC HEADER	.1" DUAL INLINE
R1-4	150K OHM	
R5-8	10K OHM	
C1-7	.1uf	MONOLYTHIC BYPASS
D1-4	746A	3.3V ZENER DIODE or equivalent
D5	1N4148	SIGNAL DIODE
PCB	NMIS-7041 PCB	REV 1.0
3x16	JUMPER PINS	BERG STYLE .1" CENTER JUMPERS
16	JUMPER SHUNTS	BERG STYLE .1" CENTER SHUNTS

NMIS-7041 Parts List Rev 1.0





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