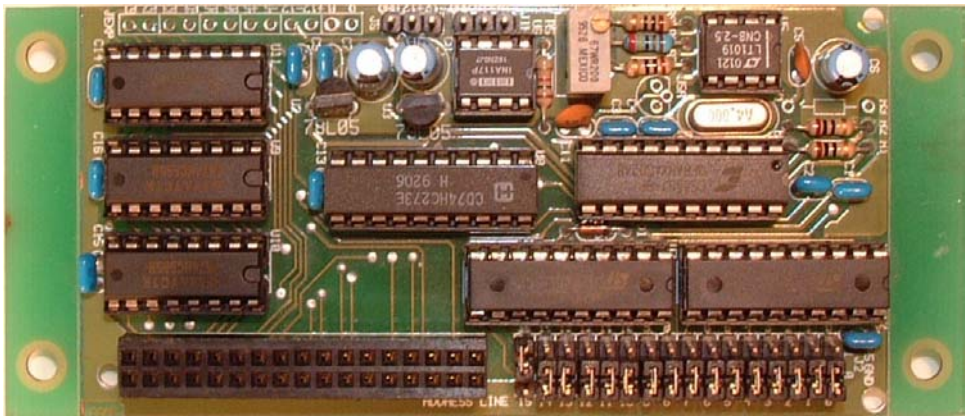
NMIS-L-4010

16-BIT ADC CARD



Covers: NMIS-L-4010 Rev. 1.0 & 1.1

GETTING STARTED

The NMIS-L-4010 Analog-to-Digital Converter Card provides a JEDSTACKTM computer system with continuous 16-bit readings of a single channel analog input. It is ideal for measuring low frequency signals (10 Hz) representing physical, chemical, and biological processes. The Burr-Brown INA117 is used as a unity gain differential amplifier and input buffer. It provides momentary 500V input protection, and can reject ñ200V common mode inputs. If galvanic isolation is not essential, this gives the functionality of isolation amplifiers and isolated input-side power supplies without the high cost normally associated with them. The Crystal Semiconductor CS5501 (or equivalent) Analog-to-Digital Converter takes 4000 readings per second and applies on-chip digital filtering (6 Pole Gaussian Low Pass, 10 Hz).

To make use of the NMIS-L-4010 requires board configuration, physical installation and the addition of the necessary software. The remainder of this section deals with these steps in greater detail. The user will probably want to read this section once, scan at least the Circuit Description and Programming chapters before taking any action, then return again to this section andfollow the suggested installation procedure. Afterwards, the other sections can provide more detail on the board's design and mechanical mounting, and on troubleshooting when things don't go quite right.

A few moments spent examining the NMIS-L-4010 will be useful. The 2x4 inch format of the NMIS board series determines the physical outline of this board. Close observation of the board reveals the following features:

The heart of the NMIS-L-4010 is the CS5501 Analog-to-Digital Converter. It is supported by the INA117 precision differential amplifier, and an LT1019 2.5V reference.

J5 is the analog input supply connector. These supplies may range from +/-7V to +/-18V. They go directly to the INA117, and are regulated to +/-5V for the converter's supplies and the 2V5 reference.

JEXP is a twelve-pin connector to facilitate future expansion.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5 Volt power and ground.

A 74HC138 is used to generate timed chip selects which operate the bus interface (a 74HC374 and two 74HC595's).

Address decoding is accomplished by two octal comparators, 74HC688's, and 14 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-L-4010 occupies four address locations. This area in the 64K address space of the JEDSTACKTM processor's bus can be selected by correct jumper placement and will inhibit other use of these addresses by the processor. The lowest two bits are ignored in comparison, so their jumpers need not be set, and only addresses divisible by 4 should be chosen.

To install the NMIS-L-4010, the following procedure is suggested:

1. Select the base address (or accept the factory default).
2. Set the jumpers for the selected address (or check the factory default).
3. Before installing the board, verify that the selected address is free of memory conflict.
4. Turn off the power to the system.
5. Install the board by connecting the VSC.
6. Verify correct alignment visually.
7. Connect the analog supplies and a voltage source for conversion.
8. Turn on system power.
9. Verify the presence of the board in memory.
10. Select or create the program or program segments to be used.
11. Install the program or program segments.

WARNING!

High Voltages may be present at the inputs of this board! Most of the other NMIS Series boards have only low voltages on them. If you are reading this to find out about maintaining a system, your first interest should be in finding out exactly what characteristics (specifically possible common-mode voltages) are to be expected of the analog input. Due care should then be taken around the small area between the input jack and the INA117.

1) Selection of the base address for the board will depend greatly on the processor card being used, system design, and how many other boards are being used in the system:

The most popular CPU that can use the NMIS-L-4010 is the F68HC11-based NMIS-L-0021, NMIX/T, and NMIY-series, or 8051-based NMIS-L-0016, NMIX/T, and NMIY-series. Although there could probably be valid reasons for mapping the Analog-to-Digital Converter Card almost anywhere in the 64K byte address space, a likely place would be in the B000 hex area above the registers. B040 hex, the next address up, could be most convenient for the first 2x4TM card in a system.

On the other hand, an address above the EEPROM would have more merit for both the NMIS-0021 CPU and the NMIX-0022 alike. The NMIX-0022 CPU's have a 68HC24 PRU that is loosely decoded in the B000 through B7FF hex range, and the EEPROM extends from B800-BBFF. Setting cards between BC00 and BFFF is good practice. This permits over a thousand locations, while having minimal impact on the greater goal of leaving large areas of contiguous memory unbroken.

The older NMIX-0011 and NMIX-0012 CPU's can use the NMIS-L-4010, but these boards use the 0100 hex page for I/O devices. In this case an address such as 0110 hex would be appropriate.

2) Once an address is selected, it is easy to set the jumpers. Convert the address to a binary number and, starting left to right, set the jumper corresponding to each bit in the binary number to a "1" or "0". Refer to Appendix A for graphic examples.

3) The factory default address setting for the NMIS-L-4010 is 8000 hex and will be used in these examples. Substitute the corrected value in place of 8000 hex if the base address has been modified. It is advisable to verify that the selected addresses are free of memory conflicts before installing the board.

First, look at the memory addresses the ADC Card will occupy to ensure that no other devices are already mapped there. This could cause interference called bus contention. If no problems are apparent on the design level, attempt to dump a memory range around the selected address. If no memory or other circuitry interferes, this will normally result in an ascending number pattern as is shown below in a dump by an F68HC11.

COLD
Max-FORTH V3.x
HEX OK
8000 40 DUMP
8000 0 1 2 3 4 5 6 7 8 9 A B C D E F
8010 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
8020 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F
8030 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F
OK

4-7) Turn off power to the system and carefully align the 34 Pin Vertical Stacking Connector (VSC) with the board to be mated. The VSC is a "straight through" connector so the NMIS-L-4010 can be added to the top or the bottom of a board stack. It's easy to get a misalignment, so double check the fit by looking at the connector from all four directions for pins that are not correctly mated. Use the provided hex standoffs (4-40, male/female screw, 3/4" brass), in the hole adjacent to the VSC to increase mechanical rigidity.

8-9) The ADC chip should be powered before its inputs are driven, so connect the Analog supplies to J5 next. +/-7 to 18V are required, at (typical) 7mA. (Use of the SLEEP* line can cut this to about 2mA.) To verify operation, turn the system power on and dump a range including the selected base address. The phantom pattern above should be disrupted for the two bytes which return the board's measurement. No other addresses can be read, and no others should change.

10-11) Testing Analog operation, calibration, and at least a bit of programming can not be separated. With a 2V5 reference input and unity gain in the INA117 input buffer, the CS5501 should be measuring a signal of at least 2V minimum span for best accuracy, but operation can be veriified and some familiarity with the card gained by trying to measure the voltage on an old 1V5 battery. Arrange things so that it is easy to connect the battery across the inputs in either direction.

```
(  Let us assume you are using a 6811 MAX which has some off-chip RAM: )
COLD
HEX
400 DP !    ( Start compilation on page 04XX: )

: IS CONSTANT ;

8000 IS PORT              ( Our standard default address )
HERE IS RAM-PORT  ( MCU must be able to keep track of )
1 ALLOT                   (     control register contents.    )

: ADC!  DUP RAM-PORT C!  PORT C! ;  ( Always do both at once )

: ADC?  RAM-PORT C@ ; ( To read  back  port status )

:  ADC@ PORT @ ;          ( To read measured value    )

01 IS CAL*          ( Bit Patterns ...   Calibrate  Command Line )
02  IS  BP/UP*      ( Bipolar/Unipolar Line )
10 IS AWAKE       ( Power  Miser  Control Line )

: CAL!   ADC? CAL* OR ADC!  ADC? CAL* NOT AND ADC! ;
( This will request a calibration, type as preset by SC1 and SC2 )

AWAKE  BP/UP*  OR   ( Form Compound Bit Pattern )
ADC!                        ( Preset for Bipolar,  Self-Cal,  and Awake )
CAL!                        (  This  takes  750 msec. )
(  This  leaves  a  reading  of  0000  representing  -2V5, )
(  and  FFFF  representing  +2V5  )

 : DELAY   100 0 DO LOOP ;

: TEST    CR   BEGIN   ADC@  8 U.R  DELAY
       ?TERMINAL  UNTIL     KEY DROP ;

TEST
(  Except  for  nicads,  any  somewhat  live battery should  return   )
(  values  below  4000  and  above  C000  depending  on   polarity. )

(  If  you  can  get  these  results,  the  NMIS-L-4010 is now calibrated, )
(  running,  measuring,  and communicating  as  it  should. )
```

CIRCUIT DESCRIPTION

The NMIS-L-4010 Card is designed to stack on single-board VSC computers. These now include the 2x4"sTM NMIS Series, the "100 Squared"TM NMIX, and the "Generic Target Computer"TM NMIT Series (with the Vertical Stacking Connector added to the latter). The "JEDSTACK"TM provides interface signals to the board including address lines, data lines, control lines and 5 Volt power and ground. The fast HC devices allow access times approaching 90nS.

The active address locations are user-set by the arrangement of addressing jumpers. Each address line can be sensed for high or low condition. (Jumpers were used rather than switches for power savings reasons. Generally, schemes that employ switches use pull-up resistors that are switched to ground for a "0", and left open for a "1". When the switches are closed, the resistors are hooked from the +5V rail to ground. While this gives the comparator inputs a suitable logic level "1" or "0", the selection of "0" wastes power. Our design, using jumpers, hooks the CMOS comparator inputs directly to +5V or Ground without wasting power.)

Two 74HC688 (U1 and U2) octal comparators decode the 16 address lines (A15-A2, ignoring A0-A1) gated by one control line (AS' for F68HC11 systems, CSEX' for R65F11 systems) in order to select four active locations out of a 64K address space. The 74HC138 uses this select for its negative enable and the E clock for its positive enable. (The "E" clock is necessary for correct timing information when using a 6500 or 6800-type processor on the JEDSTACKTM bus.) The address inputs to the 74HC138 include the R/W line. The use of the R/W line allows generation of separate selects on board for read and write accesses.

Three decoded chip selects, now containing direction and timing information, go to the bus interface chips. The ADC chip is directly controlled by six bits of a 74HC374 octal latch which responds to writes of the base address. (Refer to the next section for more details.) A pair of 74HC595's look to the ADC chip like a sixteen-bit shift register feeding a latch. On their bus side, reads of the base address return the MSByte of the current measurement, and reads of the next address return the LSByte. (This order is correct for Motorola MCU's.)

The remaining five selects are taken to JEXP1-5, along with the INA117 output/5501 input, four supplies and two grounds.

The rest of the chips handle the analog functions. There are two TO-92 transistor-size regulators, an L1019 Voltage Reference, the INA117 input buffer, and the A-D Converter itself. The LT1019 precision reference supplies 2V5 to the ADC with (typical) 20 ppm accuracy. The INA117 precision unity-gain differential amplifier can be adjusted for maximum Common Mode Rejection Ratio via R8. It features .001% linearity and 200KHz bandwidth.

The ADC itself is a CS5501 charge-balance converter, incorporating a delta-sigma analog modulator and a six-pole Gaussian digital filter. The converter is enhanced with on-chip calibration microcontroller and RAM, serial interface logic, and a clock generator. It continuously provides true 16-bit measurements, stable in all bit positions and with no missing codes, at 4KHz. It boasts .003% linearity, 0 to 70øC. (An optional configuration is available with .0015% linearity, -40 to 85ø C.) It is a complex, high-precision device, capable, for example, of dropping filtering frequency by running at 1% of the speed used on a stock board. For demanding applications, the user is urged to refer to Crystal Semiconductor's own documents about the chip.

The ADC MODE pin is tied high, which causes it to operate in Synchronous Self-Clocking mode, perfectly suited to the 74HC595's. Its six other control pins are driven by the latch at the base address.

REGISTER(S)

The NMIS-L-4010 Analog-to-Digital Converter has a discrete control register, a 74HC374 octal latch. Six of its outputs go to pins used to control the ADC:

01 IS CAL* (Bit Patterns ... Calibrate Command Line)
02 IS BP/UP* (Bipolar/Unipolar Line)
04 IS SC2 (Calibration Mode Line)
08 IS SC1 (Calibration Mode Line)
10 IS AWAKE (Power Miser Control Line)
20 IS SELECT* (ADC CS* Line used for SPI-style serial.)

Changing the SELECT* bit will not be found useful, given the board wiring. It should be kept low.

The AWAKE bit should be kept high when the ADC board is in use. Taking it low will save 5mA of demand on the analog supplies, by shutting down all but the calibration memory of the CS5501.

SC1 and SC2 control which type of calibration will be done next. They should be treated in unison with BP/UP*, which determines whether input measurements are to be signed. All three bits take effect only when CAL* goes from one to zero. See code fragments elsewhere in this document for CAL!, an example of this sequencing.

Four calibration sequences may be started by toggling CAL* :

If both SC1 and SC2 are zero, the ADC will self-calibrate in about 750 msec. It takes its AGND input for zero, and VREF for full-scale. Full-scale measurements are used to calculate slope, or System Gain.

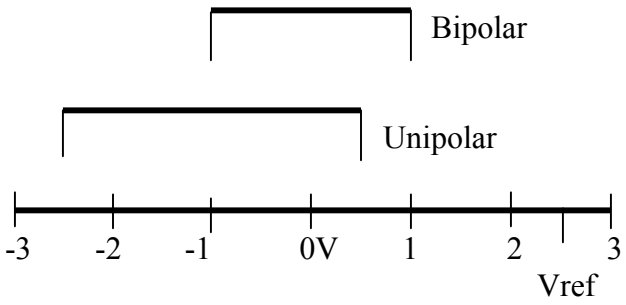
If SC1 is high and SC2 is low, the ADC calibrate out errors in System Offset only, in about 525 msec. It reads an input signal which must remain steady and becomes measurement zero. It then takes VREF for full-scale.

If both are high, a two-step calibration is begun. The input voltage is read to set measurement zero in about 250 msec.

The second step is started with SC1 low and SC2 high. The input voltage is read to set full-scale in about 250 msec. After this, the previous step can be repeated as desired to reposition the zero reference point (offset).

If it is easy to have your voltage source deliver its minimum and maximum readings, the two-step calibration allows you to have the benefit of all 16 bits of accuracy applied to the exact voltage range in question.

Possible Range of System Offset Adjustments



PROGRAMMING

As a peripheral device, the NMIS-L-4010 could not be much simpler: two parallel input ports and a single control register. Six control lines on the CS5501 can be set by a byte write to the latch at the board base address, accomplished in high level FORTH by the byte-oriented **C!** .

When writing software for applications using the board, it is important to remember there is no read back of this control register. In practice this means that it may be necessary to retain in RAM an additional image of the data written to the latch. The pattern can then be read from RAM, edited, and rewritten into both the RAM variable and the latch.

This technique is used in the progamming examples when they set calibration and polarity, because a downward transition on bit 0 is used by the ADC chip to read in data on bits 1, 2, and 3. These should hold stable while bit 0 changes. (The status of the only other usable control, the SLEEP* or AWAKE line, is reflected in the 4th bit of the RAM copy.)

The ADC and shift registers run continuously to keep a fresh 16- bit measurement ready, so the only complication in reading is to remember that the Most Significant Byte is read from the board base address. If you are using a processor of the other byte sex, swap the bytes after a word read. Alternatively, fix short wires to pins 10 and 11 of a spare 74HC138 and exchange their connections in the socket.

Some useful program segments are shown in "Getting Started".

BOARD MOUNTING

The NMIS-L-4010 has three mounting holes. One, the main mechanical mounting hole, is in the corner nearest the 34-pin Vertical Stacking Connector. The other two holes, used for alignment, are in the upper left and upper right corners. Each hole is drilled at .110 inches. This allows passage of a 4-40 screw shaft.

If additional 2x4"sTM are to be used, they may be stacked above or below, as desired, on the female or male side of the Vertical Stacking Connector respectively. A simple hex 3/4 inch standoff with a male screw on one end and a female threaded hole on the other is the ideal interboard support device. The Vertical Stacking Connector was designed to work with this size spacer, giving reliable board-to-board connection.

The length of the standard spacer, .750 inches, plus the board thickness, .061 inches, gives a nominal board-to-board spacing of .811 inches. If an exact spacing of .800 inches is desired (some standard mounting hardware has .800 inch mounting board guides), .011 inches of the mounting surface at the female end of the soft brass standoff can be removed by mill or metal file.

Only the mounting hole near the Vertical Stacking Connector has sufficient clearance around the hole to allow for the head of a screw or the flats of the standoff to rest on. The trace closest to the hole is GND. All 2x4"sTM are designed with this same convention.

The two holes at the other end of the board can be used for alignment pins, but do not have sufficient clearance to allow the use of a large-head screw. (Normally, all 2x4"sTM follow a convention of keeping these two "locking holes" clear. If there is sufficient design reason, other family boards may pre-empt that space. This could influence stacking order and hardware layout of multi-board systems.)

The extremely small size of the boards means there are no guaranteed limits on how close to the edge of the 2x4"sTM components will be placed. Board guides will be difficult to use and designs should take this into account. They may be accept able if nonconductive and very shallow. However, the main mounting hole remains the best point of support.

TROUBLESHOOTING

For the job it does, the NMIS-L-4010 is a fairly straightforward board. Three groups of three chips each handle the functions of address detection, data storage, and analog processing.

The first sign of trouble would be results as displayed in Step 3 of "Getting Started" after completing Step 9. The simplest and most likely explanation is that the address selectors are not set for the base address used in the program. Confirm the jumper pattern very carefully. If the board still fails to read anything from the 74HC595's, check the VSC connections and the 74HC688's. Use a probe or scope to verify that the base address select line at Pin 4 of the 74HC138 responds when the correct address is read. Replace the 74HC688's if not.

If it does, check the two lines that ask the 74HC595 to send data. Pin 10 of the 74HC138 should respond to reads of the low address (MSB), and Pin 11 to reads of the high address (LSB). Replace the 74HC138 if not.

Next suspect the 74HC595 latched shift registers; they ought to at least be able to drive a signal on to the bus when selected. Try replacing them. If that doesn't work, you have reached Dead End #1.

Once the board shows in memory, the next objective is to confirm correct control signals are going to the ADC chip. Pin 15 of the 74C138 should notice when the processor writes to the base address. If this works, the 74HC374 outputs should reflect the data byte written, as described in the "Register" section. Make sure that Pin 11 of the ADC chip is high! Otherwise the converter is sleeping. If it is awake and Pin 19 (the serial clock) is not changing, the ADC is not sending readings.

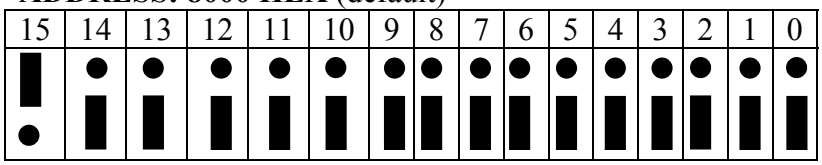
The bad news at this point is that the ADC is under suspicion. The good news is that the most likely problem is that its digital power is taken from the board analog supply, and it is easy (though not good for the ADC) to forget to connect that up. See if pin 10 is showing the 2V5 reference. If it does, short of replacing the CS5501 itself, you have reached Dead End #2.

If there is power, some kind of readings should be getting to the processor. Run through the Self-Calibration routine from "Getting Started". See what happens to JEXP Pin 6 (which has the Buffer output/ADC input) when the famous old battery is connected and reversed. If this pin does not track, the INA117 must have been damaged. If it tracks, and processor readings do not, you have reached Dead End #3.

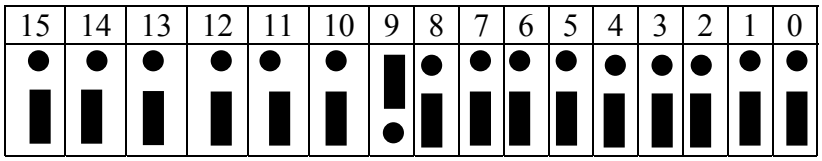
Dead End: There is little further service that can be performed by the customer. Contact the factory for repair if these suggestions do not help.

JUMPERS

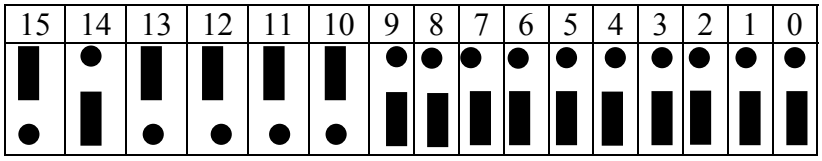
ADDRESS: 8000 HEX (default)



ADDRESS 0200 HEX



ADDRESS BC00 HEX



Note: Jumpers 0 and 1 are not read by the comparators. Valid addresses are divisible by 4

PROGRAM SEGMENTS

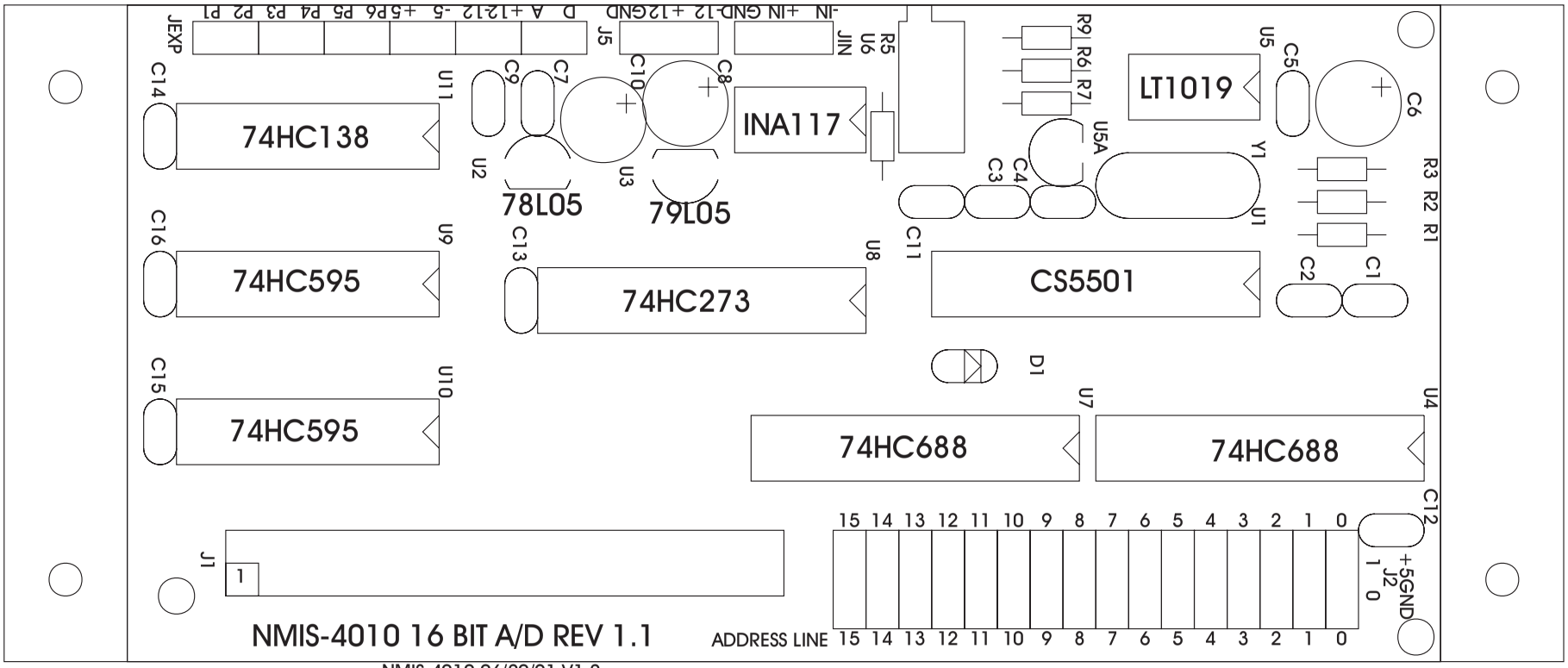
```
( This example picks up from the code in "Getting  Started"  just after )
(  ADC@  is defined,  now incorporating all the control lines and doing )
( a hands-on calibration to external zero  and  full-scale  voltages. )

01 IS CAL*        ( Bit Patterns ...  Calibrate Command Line )
02 IS BP/UP*      ( Bipolar/Unipolar Line )
04 IS SC2         ( Calibration Mode Line )
08 IS SC1         ( Calibration Mode Line )
10 IS AWAKE       ( Power Miser Control Line )
20 IS SELECT*     ( ADC CS* Line used for SPI-style serial. )

: CAL!   ADC? CAL* OR ADC!  ADC? CAL* NOT AND ADC! ;
( This will request a calibration,  type as preset by SC1 and SC2 )

: STEP1
     SC1 SC2 OR  AWAKE OR    ( Form Compound Bit  Pattern )
     ADC!                    ( Preset for Unipolar,  Two-Step Cal, Awake )
     CAL!  ;                 ( Step One  takes  250 msec. )

: STEP2
     SC2     AWAKE OR        ( Form Compound Bit Pattern )
     ADC!                    ( Preset for  Unipolar,  Step  Two, Awake )
     CAL!  ;                 ( Step Two takes 250 msec. )

: EXT_CAL
     CR  ." Connect Zero Voltage Source.   Press  any  Key  when  Ready "
     KEY  DROP   STEP1     ( This voltage will leave a reading of 0000 )
     CR  ." Connect Full Scale Voltage Source.   Press  any  Key when Ready"
     KEY  DROP  STEP2  ;  ( This voltage will leave a reading of  FFFF )

EXT_CAL
```

```
( Maintain a large-format binary representation of the current )
( measurement across the top of the terminal screen.  Assume only  )
( that ANSI clear_screen and cursor_home sequences are supported.  )

: ESC-IT      1B EMIT  5B EMIT   EMIT ;
: CH  ( Cursor_Home! )          48 ESC-IT  ;
: CS  ( Clear_Screen! )    CH     4A ESC-IT  ;

: LIGHT-BIT    ." ***"  SPACE ;
: DOUSE-BIT    4 SPACES  ;

: DISPLAY_BIT   ( mask --- mask )
    DUP  ADC@ AND   IF LIGHT-BIT ELSE DOUSE-BIT THEN  ;

: SAMPLE_LINE
      8000 BEGIN  DUP WHILE ( mask )  DISPLAY_BIT  2/ ( next_mask )
      REPEAT ;

: SAMPLE
      4 0 DO  CR  ( Display on screen lines 1 to 4 )    SAMPLE_LINE
      LOOP  ;

:  WITNESS     BEGIN   CS   SAMPLE    ?TERMINAL UNTIL   KEY DROP ;

WITNESS
```

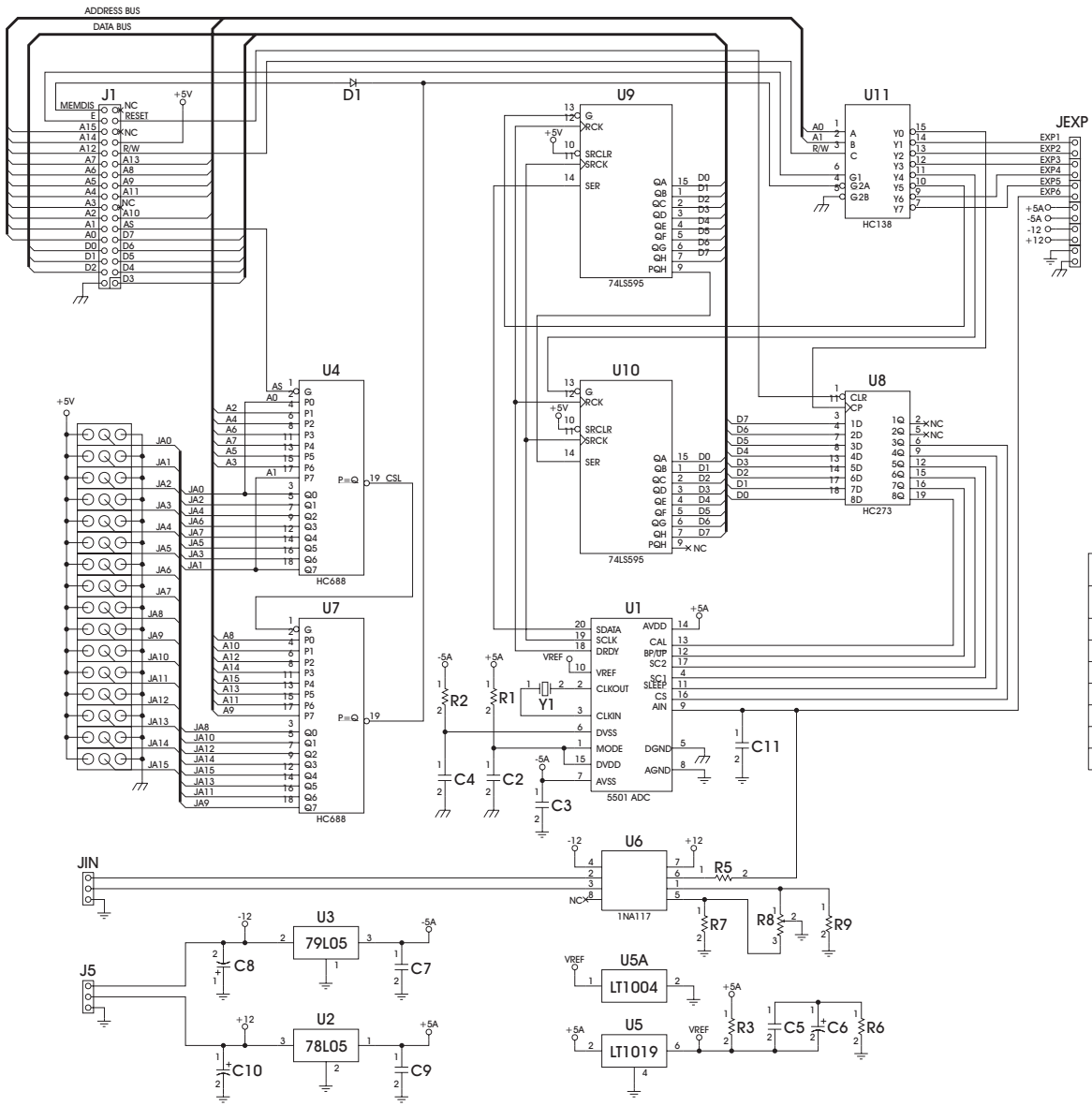
PARTS LIST

NMIS-L-4010 16 BIT A/D CONVERTER PARTS LIST

PART#	GENERIC	DESCRIPTION
U4,7	20 PIN SOCKET	
	74HC688	OCTAL COMPARATOR
U11	16 PIN SOCKET	
	74HC138	3 TO DECODER
U9,10	16 PIN SOCKET	
	74HC595	8-BIT SERIAL-INPUT/SERIAL OR PARALLEL-OUTPUT
U8	20 PIN SOCKET	
	74HC273	OCTAL D FLIP FLOP
U1	20 PIN SOCKET	
	CS 5501-BP	16-BIT A/D CONVERTER
U2	78L05	+5V VOLTAGE REGULATOR
U3	79L05	-5V VOLTAGE REGULATOR
U5	LT1019	VOLTAGE REFERENCE
U6	1NA117P	DIFFERENTIAL AMPLIFIER
J1	34-PIN VSC HEADER	.1" DUAL IN-LINE
C1-4,7,9, 12-16	.1uf	MONOLITHIC BYPASS
C5	100 PF	
C11	1000 PF	
C8,10	10 UF	
D1	1N4148 OR 1N914	SIGNAL DIODE
R1,2,7,9		RESISTORS
PCB	NMIS-L-4010 PCB	REV 1.1
JA0-15	3x16 JUMPER PINS	BERG STYLE .1" CENTER JUMPERS
	16 JUMPER SHUNTS	BERG STYLE .1" CENTER SHUNTS
JIN,J5	3x1 JUMPER PINS	BERG STYLE .1" CENTER JUMPERS



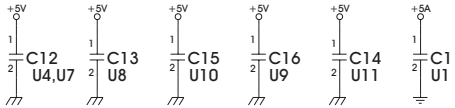
NMIS-4010 06/20/91 V1.2



TABLE

SYMBOL		SUPPLY & GROUND PINS					
REFDES	DEVICE	+12	-12	+5V	+5A	DGND	AGND
U4	74HC688	-	-	20	-	10	-
U6	1NA117	7	4	-	-	-	-
U7	74HC688	-	-	20	-	10	-
U8	74HC374	-	-	20	-	10	-
U9	74LS595	-	-	16	-	8	-
U10	74LS595	-	-	16	-	8	-
U11	74HC138	-	-	16	-	8	-

DECOUPLING CAPACITORS



New Micros, Inc. COPYRIGHT 1991		16-BIT ADC CARD
APPROVALS	DATE	TITLE NMIS-L-4010
DRAWN CIBI-ARDY	061491	
CHECKED		SIZE D DWG NO. ABR02 REV
FINISH		SCALE SHEET 1 OF 1