NMIS-L-3000

32-BIT INPUTS & 32-BIT OUPUTS CARD

Getting Started

The NMIS-3000 32-In 32-Out Card provides a JEDSTACK™ computer system with 32-bits of latched outputs and 32-bits of latchable inputs. The inputs and outputs are arranged to easily connect to control points. Two 34 conductor ribbon cable, or 68 individual wires can be used to connect to the 64 I/O points with 2 power and 2 ground connections. The NMIS-3000 is 2" x 4". The NMIL-3000 is identical to the NMIS-3000, except for being slightly longer. Mounting tabs are added at each end of the board. The NMIL-3000 is, therefore, 2" x 4.75". References to the NMIS-3000 also apply to the NMIL-3000, with exception of references relative to these extra mounting tabs.

To make use of the NMIS-3000 requires board configuration, physical installation and the addition of the necessary software. The remainder of this section deals with these steps in greater detail. The user will probably want to read this section once, then scan the Circuit Description and Programming chapters before taking any action, then again return to this section and follow the suggested installation procedure. Finally, the other sections will tell more on the board's design and mechanical board mounting.

A few moments spent examining the NMIS-3000 will be useful. The 2x4 inch format of the NMIS board series determines the physical outline of this board. (The NMIL-3000 has an active component area of 2x4 inches, but also has two mounting tabs, giving an overall size of 2x4.75 inches.) Close observation of the board reveals the following features. Connector J1 and J2 runs along the left side of the board. The individual I/O points are labeled on the board, grouped into ports of 8 lines each, Ports A through H. Next to these connectors runs a vertical row of 8 bit latches. Four are 74HC573's which are used as input gates with the optional externally controlled latching and four are 74HC574's which are used as output latches. Further to the right of the latches are bus interface chip. A bi-directional transceiver, 74HC245, buffers the data bus from the loads of the 74HC573 and 74HC574's. A 74HC32 is used in conjunction with a 74HC138 to generate the chip select and timing information to operate the latches and drivers. A Vertical Stacking Connector in the lower, right-hand corner (top view) provides connections to the processor's address and data bus, control signals, 5 Volt power and ground. Address decoding of the I/O chip's space in memory is accomplished by two octal comparators, 74HC688's, and 16, two position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-3000 occupies 4 addresses. Any 4 byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.

To install the NMIS-3000, the following procedure is suggested:

1) select the base address (or accept the factory default)
2) set the jumpers for the selected address (or check the factory default)
3) set the Jumper "A" for normal (+5V) or latched (external signal) operation
4) set the Jumper "B" for normal (ground) or controlled drive (external signal) operation
5) set the Jumper "C" for processor type
6) verify the selected address is free of memory conflict before installing the board
7) turn off the power to the system
8) install the board connecting the VSC
9) verify correct alignment visually
10) turn on system power
11) verify the presence of the board in memory
12) select the program or program segments to be used
13) install the program or program segments to be used

Selection of the base address for the board will depend greatly on the processor card being used, system design, and how many other boards are being used in the system. For instance, the most popular CPU to date that can use the NMIS-3000 is the F68HC11 based NMIS-0021. Although there could probably be valid reasons for mapping the 32 Bit I/O almost anywhere in the 64K byte address space, a likely place would be in the B000 hex area above the registers. If no additional 2x4"s™ cards were in the system, B040

hex is a likely choice. On the other hand, an address above the EEPROM at BC00 hex would have more merit for both the NMIS-0021 CPU and the NMIX-0022 alike. The NMIX-0022 CPU's have a 68HC24 PRU that is loosely decoded in the B000 through B7FF hex range. Putting the 32 Bit I/O at BC00 would clear any possible memory conflicts there, while having minimal impact on the greater goal of leaving large areas of contiguous memory unbroken. The older NMIX-0011 and NMIX-0012 CPU's can use the NMIS-3000, but these boards use the 0100 hex page for I/O. In this case an address such as 0110 hex would be appropriate. Ultimately, this is a choice of the system designer and the practical restraints of the processor used.

Once an address is selected, it is easy to set the jumpers. Convert the address to a binary number and, starting left to right, set the jumper corresponding to each bit in the binary number to a "1" or "0". Refer to Appendix A for graphic examples.

The center pin on Jumper "A" is the latch control pin. If the input readings are to continuously follow the pins, Jumper "A" should be in the +5V position (toward the top edge, wtih VSC in lower right-hand corner, top view). To latch the inputs, Jumper "A" must be removed and an external signal provided to control the latching. If this were an output compare on the F68HC11 for instance, the state of all 32 input lines could be attained by the processor each time the counter compare caused the associated output pin to toggle low. The readings would be held until the line returned high again. When the line is high the 74HC573's are transparent, passing the pins current state directly to the processors bus.

Jumper "B" controls the output port drivers. When it is set to ground (toward the bottom edge, wtih VSC in lower right-hand corner, top view) the latches of the 74HC574's are enabled and it functions as a simple output board. When it is set to +5V (toward the top edge of the board) the drivers of the 74HC574's are disabled. Jumper "B" can be removed and an external signal provided to the center pin on Jumper "B" to control the latching.

Selecting and setting the jumper marked "C" for correct processor type is straight forward. Jumper "C" has two settings marked on the silkscreen, "65" and "80". If the processor type is a 6500 or 6800 type (such as the F68HC11) the jumper should be in the "65" position. If the processor type is a 8031 or Z80 type (such as the 8052AH) the jumper should be in the "80" position. The "C" jumper either applies the "E" clock or +5V to the chip select gating. The "E" clock is necessary for correct timing information when using a 6500 or 6800 type processor on the JEDSTACK™ bus. To determine which type processor is which, check the memory interface signals. If the processor itself has a RD and a WR line, it is an "80" type. If the processor has a R/W line and a clock signal such as E or 02 (pronounced phase two), it is a "65" type.

The factory default address setting for the NMIS-3000 is 8000 hex and will be used in these examples. Substitute the corrected value in place of 8000 hex if the base address has been modified. It is advisable to verify the selected address is free of memory conflicts before installing the board. First look at the memory addresses the 32 Bit I/O will occupy to see if other devices are already mapped there. These could cause interference, called, bus contention. Dumping the area around 8000 will normally show an ascending number pattern if no memory interferes, as is shown below in a dump by an F68HC11.

```
COLD
 Max-FORTH V3.3
HEX OK
8000 40 DUMP
 8000  0  1  2  3  4  5  6  7  8  9  A  B  C  D  E  F
 8010 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
 8020 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F
 8030 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F
OK
```

Turn off power to the system and carefully align the 34 pin Vertical Stacking Connector (VSC) with the board to be mated. The VSC is a "straight through" connector so the NMIS-3000 can be added to the top or

the bottom of a board stack. It's easy to get a misalignment, so double check the fit by looking at the connector from all four directions for pins that are not correctly mated. Use the provided 4-40 male/female screw 3/4" brass hex standoffs in the hole adjacent to the VSC to increase mechanical rigidity. Turn the system power on and examine the memory area around 8000 hex again.

```
COLD
 Max-FORTH V3.3
HEX OK
8000 40 DUMP
 8000 FF FF FF FF  4  5  6  7  8  9  A  B  C  D  E  F
 8010 10 11 12 13 14 15 16 17 18 19 1A 1B 1C 1D 1E 1F
 8020 20 21 22 23 24 25 26 27 28 29 2A 2B 2C 2D 2E 2F
 8030 30 31 32 33 34 35 36 37 38 39 3A 3B 3C 3D 3E 3F
OK
```

Notice the first 4 locations now have different values. These are the registers of the 74HC573's chips. Their contents will, of course, vary depending on the power up settings that happen to occur in the chip and what external connections are doing to the inpur pins. If the ascending pattern has not changed, the processor can not "see" the NMIS-3000 in its memory map. Recheck the address jumpers for proper settings and the VSC for proper connection.

The NMIS-3000 is now running and communicating as it should.

Circuit Description

The NMIS-3000 32-In 32-Out Card is designed to stack on the 2x4"s™ NMIS Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The "JEDSTACK"™ provides the interface signals to the board including address lines, data lines, control lines and 5 Volt power and ground. The fast HC devices allows access times approaching 90nS.

The addressing of the octal latches on the NMIS-3000 is sensed by two 74HC688 (U1 and U2) octal comparators that decode the 14 address lines (A15 - A4) and one control line (AS for F68HC11 systems, CSEX for R65F11 systems) to select only four active locations out of a 64K address space.

The address locations where the card is active is user set by the arrangement of addressing jumpers. Each significant address line can be sensed for high or low condition. (Jumpers were used rather than switches for power savings reasons. Generally, schemes that employ switches use pull up resistors that are switched to ground for a "0" and left open for a "1". When the switches are closed this means the resistors are hooked from the +5V rail to ground. While this gives the comparator inputs a suitable logic level "1" or "0", the selection of "0" wastes power. The design using jumpers hook the CMOS comparator inputs directly to +5V or Ground without wasting power.)

When one of the four set addresses is selected by the processor, the 74HC688's generate a chip select to the 74HC138. This signal is also coupled back on the VSC via diode D1 to the MEMDIS pin. Additionally this signal is OR'ed with Output Enable to create the signal that reverses the 74HC245 bus transceiver and causes it to drive data back to the processor during a read.

The 74HC138 uses this chip select signal for its negative enables and the output of Jumper "C" for its one positive enable. Jumper "C" will either provide a constant high if set for "80" type processors, or the "E" clock if set for 6500 and 6800 type processors. The "E" clock is necessary for correct timing information when using a 6500 or 6800 type processor on the JEDSTACK™ bus. If the processor type is a 6500 or 6800 type (such as the F68HC11) the jumper should be in the "65" position. If the processor type is a 8031 or Z80 type (such as the 8052AH) the jumper should be in the "80" position.

The address inputs to the 74HC138 include two real address lines, A0 and A1, and the R/W' line. The use of the R/W' line allows selection between reading of the input latches or writing the output latches. The eight decoded chip selects go to the latches, four to the 74HC574 output latches and four to the 74HC573 input latches.

The 74HC573's and 74HC574's are connected to the Data Bus by way of the 74HC245. The 74HC245 acts as bus buffers, limiting the load placed on the Data Bus to only one HC load (rather than eight). This increases the number of boards that can be put on the system than otherwise due to fan out limitations. By way of this bus driver the 74HC573's send data to the processor and the 74HC574's accept data from the processor.

The drivers on the 74HC574's are controlled by the signal from Jumper "B". When it is set to ground the drivers on the 74HC574's are enabled. The drivers of the 74HC574's will control the level on their I/O pins (providing there is no contention from attached equipment). When Jumper "B" is set to +5V the drivers on the 74HC574's are disabled and the I/O pins are controlled by whatever external devices may be driving them.

The center pin on Jumper "A" is the 74HC573's latch enable. When the line is high the 74HC573's are transparent, passing the I/O pins' current state directly to the processor. Jumper "A" can be removed and an external signal provided to control the latch enable. When the line is high, the 74HC573's are transparent. When the line goes low the readings are latched at their state at the time. They will continue to be read in that state despite any changes on the external I/O pins until the line returns high again.

Output drive capability of the 74HC574 list a sink and a source current of 25 mA. at normal 5 volt operation. Worse case minimums at 25 degrees C with a 4.5 Volt supply show a sink current capability of 17 mA. at an output voltage of 1.5 Volts and a source capability of 15 mA. at an output voltage of 3.0 Volts. (Caution: The total current rating for the package is considerably less than the sum of all the rated drivers. This means trying to sink all the drivers at once at full current is beyond the total system rating for the part.)

When driving other logic, the HC outputs have voltages of 0.1V and VCC-0.1V for an output current of 20 uA. or the equivalent of 20 HC loads. The output drives for standard drive devices are such that they can drive ten LSTTL loads and maintain the output voltage under or equal to 0.4 V across the full temperature range. The maximum rated output current given on the individual pins, as mentioned, is 25 mA.. The output short circuit currents of these devices will typically exceed these limits. The manufacturer reports outputs can, however, be shorted for short periods of time for logic testing, if the maximum package power dispassion of 500 mW is not violated.
Programming

The NMIS-3000 is a fairly straight forward I/O device with four parallel ports of eight bits each. It uses four consecutive addresses. Each address can be fetched or stored by a byte access. In high level FORTH, two addresses can be fetched or stored "at once" by using **@ and ! instead of the byte oriented C@ and C! . In C, the corresponding functions are peek() and poke(), and bytewise peekb() and** PEE**K command and set with the** POKE command.

When programming the NMIS-3000 it is necessary to know how the physical address and bit position within the address affects the addressing of each bit. Further, each bit has an assigned pin on connectors J1 or J2.

The NMIS-3000's lowest addressed port has the least significant 8 bits. The least significant bit in this location, PA0, controls pin-33 of J1. The second bit in that location, PA1, controls pin-33 of J1 and so on. After the most significant bit in that byte, PA7 controlling pin-27, the least significant bit in the next address in memory, PB0, controls output pin-28 and so on.

There is no read back provided on the output ports. The input ports and output ports share the same addresses. The address to read Port A is the same address as the one to write Port E. Instructions which perform read-modify-write instructions will not work for this configuration. A copy of the last written output value should be kept in a separate variable, if single bit modifications are desired. The copy can be read modified and then written to the output port.

Some useful program segments are shown in Appendix B.

Board Mounting

The NMIS-3000 has three mounting holes, one in the corner nearest the 34 pin Vertical Stacking Connector which is the main mechanical mounting hole, and two in the opposite corners used for alignment. Each hole is drilled at .110 inches. This will allow passage of a 4-40 screw shaft.

If additional 2x4"s™ are to be used they may be stacked above or below, as desired, on the female or male side of the Vertical Stacking Connector respectively. A simple hex 3/4 inch standoff with a male screw on one end and a female threaded hole on the other is the ideal interboard connection device. The Vertical Stacking Connector was designed to work with this size spacer, giving reliable board to board connection.

The length of the standard spacer, .750 inches, plus the board thickness, .061 inches, gives a nominal spacing board to board of .811 inches. If an exact spacing of .800 inches is desired (some standard mounting hardware have .800 inch mounting board guides) .011 inches of the mounting surface at the female end of the soft brass standoff can be removed by mill or metal file.

Only the mounting hole near the Vertical Stacking Connector has sufficient clearance around the hole to allow for the head of a screw or the flats of the standoff to rest on. The trace closest to the hole is GND on the top side of the board. All 2x4"s™ are designed with this same convention.

The two mounting holes at the other end board can be used for alignment pins, but do not have sufficient clearance to allow the use of screw. All 2x4"s™ attempt to follow the convention, maintaining these two mounting holes. If, however, there is sufficient reason to use that board space they may not always be preserved.

The extremely small size of the boards means there are no guaranteed limits on how close components will be placed to the edge of the 2x4"s™. Board guides will be difficult to use and designs should take this into account. They may be acceptable if non conductive and very shallow. The main mounting hole remains the best point of support.

This board is also available in the "long" version, the NMIL-3000. The NMIL boards have an additional mounting tab on each end, so the total board outline is 2x4.750". Each end tab is 2"x3/8". Two .156" mounting holes are centered on the tabs, .250" from the edges. Hex .250" male-female standoffs can be used to make a rigid cage-like structure with NMIL boards. Special metal mounting tabs can also be used to mount the boards perpendicular to a surface. The NMIL versions of NMIS boards add a little size, but offer extremely roughed mounting.

Troubleshooting

The NMIS-3000 is a fairly simple and straight forward board. The most likely problem encountered remains "operator error". There are a minimal number of things that could be wrong otherwise that are customer serviceable.

Check the address selectors and verify they are set for the base address used in the program. Use the memory dumps outlined in the "Getting Started" chapter. If the input registers don't appear in memory, check the VSC connections and the 74HC688's. Finally replace the 74HC688's if necessary.

If the inputs still do not appear, check the outputs with a logic probe. First be sure to configure Jumper "B" to enable the outputs. Check for all low after writing zeros to the locations. Then check for all high after writing ones (FFFF hex) to the locations. If the outputs follow what is written, the 74HC574's are working and the 74HC573's are the problem. If the outputs do work and the inputs don't, recheck Jumper "A" to see it is either strapped high or the input signal occasionally goes high to let the latched data change.

If the inputs work and the outputs don't, check Jumper "B". If it is strapped low the outputs should be enabled. If it is high they will be inhibited and can not control the pins.

The majority of the board uses surface mount technology, and there is little further service that can be performed by the customer. Contact the factory for repair if these suggestions do not help.

Jumpers

ADDRESSES 8000-8003 HEX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	o	o	o	o	o	o	o	o	o	o	o	o	o	*	*
X	X	X	X	X	X	X	X	X	X	X	X	X	X	*	*
o	X	X	X	X	X	X	X	X	X	X	X	X	X	*	*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ADDRESSES 0110-0113 HEX

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
o	o	o	o	o	o	o	X	o	o	o	X	o	o	*	*
X	X	X	X	X	X	X	X	X	X	X	X	X	X	*	*
X	X	X	X	X	X	X	o	X	X	X	o	X	X	*	*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

ADDRESSES BC00-BC03 HEX

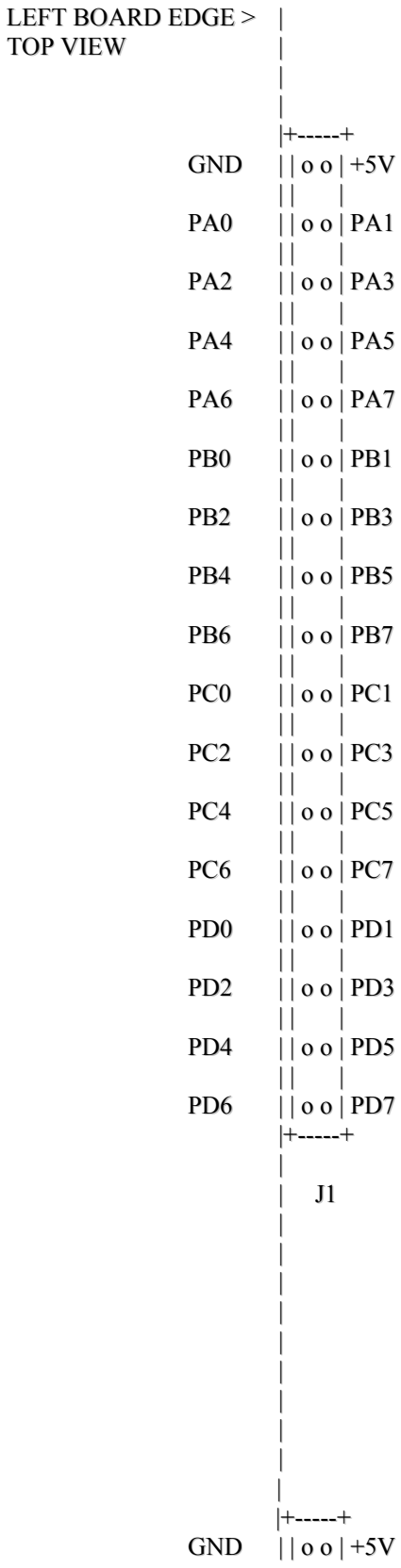
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
X	o	X	X	X	X	o	o	o	o	o	o	o	o	*	*
X	X	X	X	X	X	X	X	X	X	X	X	X	X	*	*
o	X	o	o	o	o	X	X	X	X	X	X	X	X	*	*
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

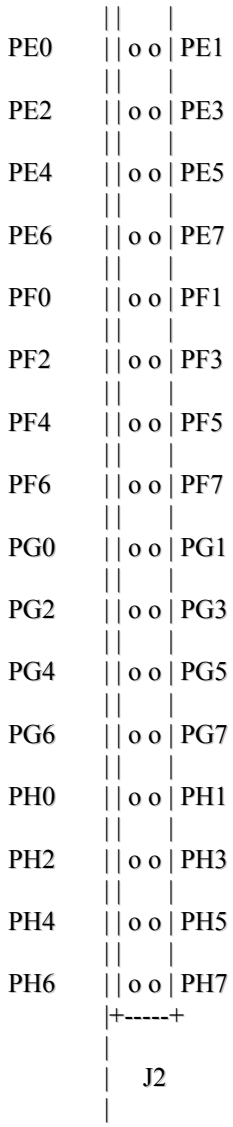
* NOTE: These are "DON'T CARE" as long as 0 or 1, will not effect base address.

Program Segments

```
COLD

FORGET TASK
HEX
( 100 1C ! ( V3.3 only
( 50 1E ! ( V3.3 only
404 DP !

: IS CONSTANT ;
8000 IS BASE-ADDRESS

BASE-ADDRESS 0 + IS PORTA
BASE-ADDRESS 1 + IS PORTB
BASE-ADDRESS 2 + IS PORTC
BASE-ADDRESS 3 + IS PORTD

BASE-ADDRESS 0 + IS PORTE
BASE-ADDRESS 1 + IS PORTF
BASE-ADDRESS 2 + IS PORTG
BASE-ADDRESS 3 + IS PORTH

: PA@ PORTA C@ ;
: PB@ PORTB C@ ;
: PC@ PORTC C@ ;
: PD@ PORTD C@ ;

: PE! PORTA C! ;
: PF! PORTB C! ;
: PG! PORTC C! ;
: PH! PORTD C! ;

: PAB@ PORTA @ ;
: PCD@ PORTC @ ;

: PEF! PORTE ! ;
: PGH! PORTG ! ;
```

I/O Connectors


LEFT BOARD EDGE >
TOP VIEW
GND
+5V
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
PC7
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
J1
GND
+5V



J1, J2 I/O Connector Pin Out

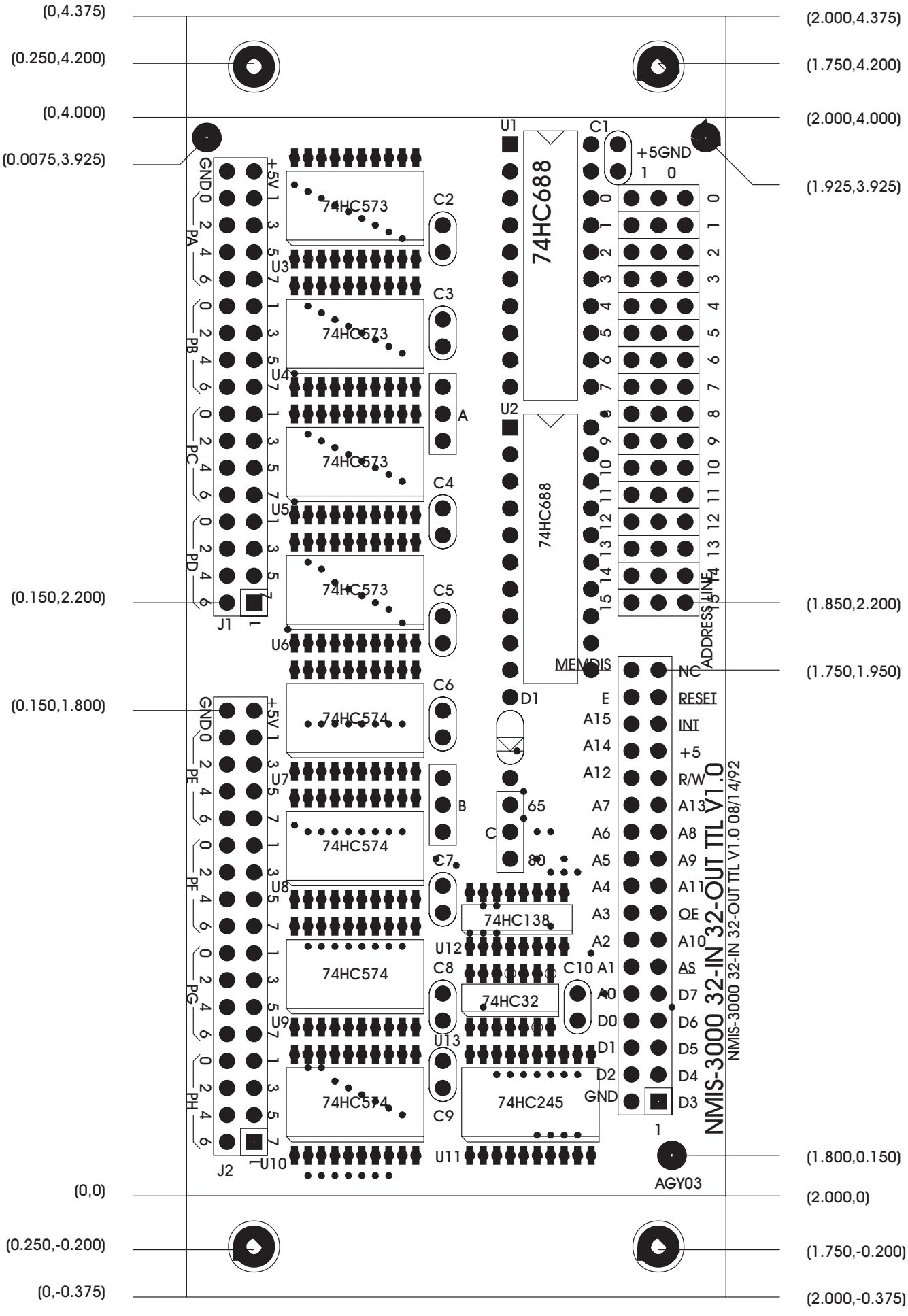
Parts List

NMIS-3000 32-IN 32-OUT PARTS LIST REV 1.0

PART#	GENERIC	DESCRIPTION
U1,2	20 PIN SOCKET	

	74HC688	OCTAL COMPARATOR
U3,4,5,6	74HC573	OCTAL LATCH - SMD
U7,8,9,10	74HC574	OCTAL LATCH - SMD
U11	74HC245	OCTAL BUS TRANSCEIVER - SMD
U12	74HC138	3 TO 8 DECODER - SMD
U13	74HC32	QUAD OR - SMD
J1	34 PIN HEADER	.1" DUAL INLINE
J2	34 PIN HEADER	.1" DUAL INLINE
J3	34 PIN VSC HEADER	.1" DUAL INLINE
C1-10	.1uf	MONOLYTHIC BYPASS
D1	1N4148 OR 1N914	SIGNAL DIODE
PCB	NMIS-3000 PCB	REV 1.0
3x16	JUMPER PINS	BERG STYLE .1" CENTER JUMPERS
16	JUMPER SHUNTS	BERG STYLE .1" CENTER SHUNTS
3x3	JUMPER PINS	BERG STYLE .1" CENTER JUMPERS
3	JUMPER SHUNTS	BERG STYLE .1" CENTER SHUNTS

NMIS-3000 Parts List Rev 1.0


(0,4.375)
(2.000,4.375)
(0.250,4.200)
(1.750,4.200)
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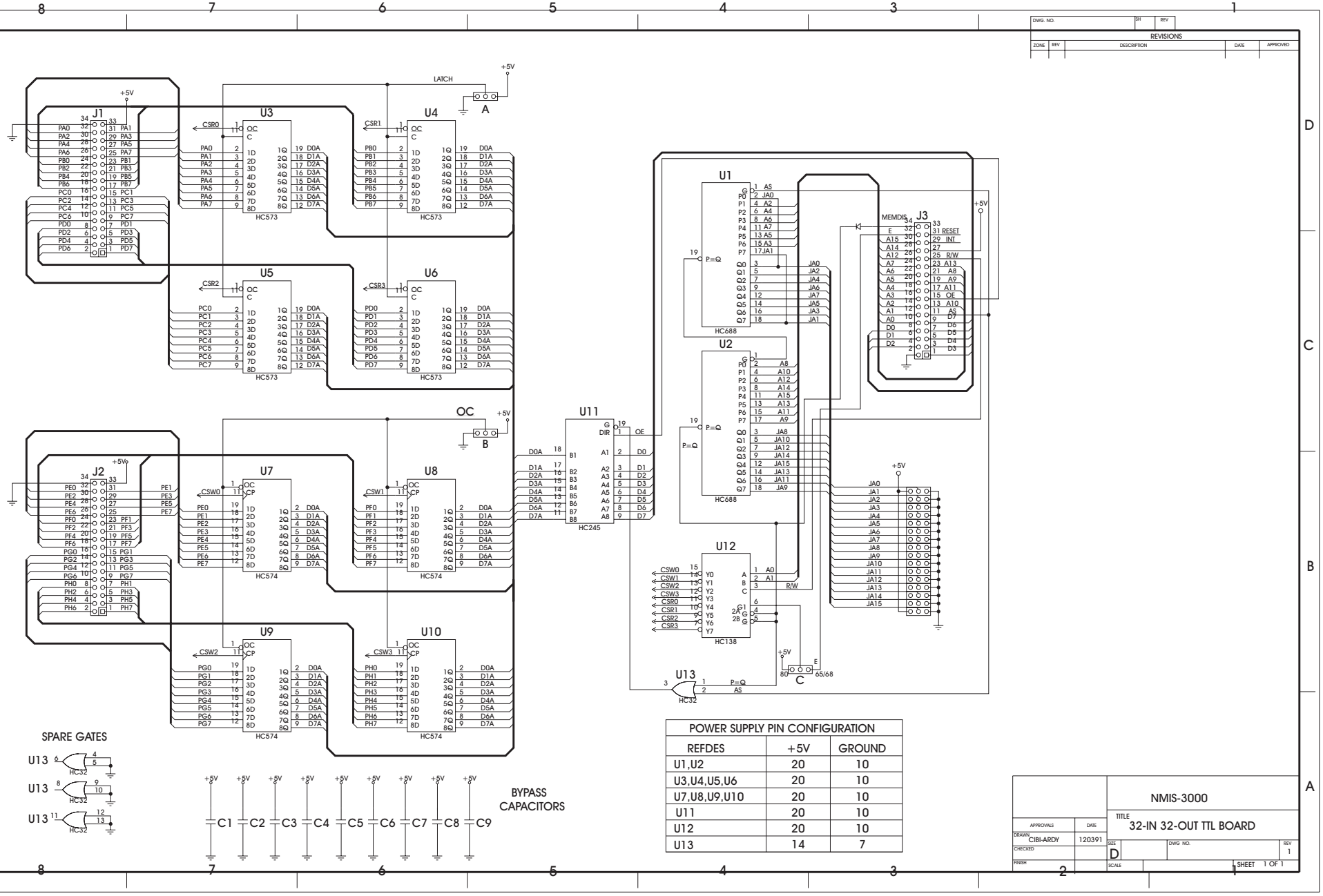
(2.000,4.000)
(0.0075,3.925)
(1.925,3.925)
(0.150,2.200)
(1.850,2.200)
(1.750,1.950)
(0.150,1.800)
(1.800,0.150)
(0,0)
(2.000,0)
(0.250,-0.200)
(1.750,-0.200)
(0,-0.375)
(2.000,-0.375)
U1
74HC688
U2
74HC688
C1
+5GND
1 0
ADDRESS LINE
MEMDIS
NC
E
RESET
A15
INT
A14
+5
A12
R/W
A7
A13
A6
A8
A5
A9
A4
A11
A3
OE
A2
A10
A1
AS
A0
D7
D0
D6
D1
D5
D2
D4
GND
D3
1
AGY03
D1
65
C
80
A
B
C2
C3
C4
C5
C6
C7
C8
C9
C10
U3
74HC573
U4
74HC573
U5
74HC573
U6
74HC573
U7
74HC574
U8
74HC574
U9
74HC574
U10
74HC574
U11
74HC245
U12
74HC138
U13
74HC32
J1
J2
GND
+5V
PA
PB
PC
PD
PE
PF
PG
PH
NMIS-3000 32-IN 32-OUT TTL V1.0
NMIS-3000 32-IN 32-OUT TTL V1.0 08/14/92



POWER SUPPLY PIN CONFIGURATION		
REFDES	+5V	GROUND
U1,U2	20	10
U3,U4,U5,U6	20	10
U7,U8,U9,U10	20	10
U11	20	10
U12	20	10
U13	14	7

APPROVALS	DATE	NMIS-3000
DRAWN CIBI-ARDY	120391	TITLE 32-IN 32-OUT TTL BOARD
CHECKED		SIZE D · DWG NO. · REV 1
FINISH		SCALE · SHEET 1 OF 1