GETTING STARTED

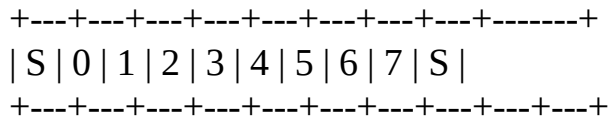
The 2x4"sTM series of computer boards were designed with low power operation and minimal size in mind. The 2x4"sTM are the perfect building blocks when designing systems or stand alone single-board computers. They were named 2x4"sTM for their size, 2 x 4 inches, and to emphasis the similarity in concept to the popular mechanical building block. The NMIS-0021 is the F68HC11 based CPU board for the 2x4"sTM board series.

The NMIS-0021, when purchased, is ready to run your dedicated application. Only the addition of your program is required in its internal EEPROM, or its battery backed RAM, or in a user supplied ROM/EPROM/EEPROM.

If you wish to download code to the processor, or interactively develop code, additional circuitry is probably needed. To "talk" to the system with a standard RS-232 terminal or a personal computer with an RS-232 port, you must have a level shifter to convert the TTL serial in and serial out to RS-232 levels. This can easily be done if you have purchased a NMII-0232 board. If you don't have a NMII-0232 board, you will need to build a level shifter. See SERIAL I/O for details on the construction of a simple level shifter. After you have your level shifter connected to the NMIS-0021, connect a terminal to the serial RS-232 DB25F connector. Most terminals should plug in directly, with a straight through cable (i.e.:: pin 1 to pin 1, 2 to 2, 3 to 3, etc.).

The terminal must have the correct bit settings. The baud rate should be set at 9600 baud for 2 Mhz systems (8 Mhz crystal), 4800 for 1 Mhz systems (4 Mhz crystal). The NMIS-0021 sends and

receives a bit protocol of one start bit, eight data bits and one stop bits.



Bit Stream

When the terminal is set correctly, and the board is provided with power, every time you cause a reset to occur the NMIS-0021 should respond with:

Max-FORTH V3.3

Seeing that message means the terminal can "talk" the NMIS-0021. Press "return" on your terminal several times. If the NMIS-0021 responds with "OK" each time, communications are established.

Now you will want to see the system do something. Type WORDS followed by a return. This will cause the system to list its entire vocabulary, some 200+ words. The listing can be stopped at any time by pressing a key, like the space bar.

When the F68HC11 powers up, it assumes nothing else on the board is working, so it defaults to its own internal RAM. As a result there is a limited terminal input buffer area (16 characters) and dictionary space. The NMIS-0021 provides external memory expansion. You now need to tell the system to move its terminal input buffer and dictionary to external memory. If the RAM is installed at 0100-1FFF (factory default for single 8K RAM) the following will accomplish that.

```
HEX
100 TIB !
50 TIB 2+ !
200 DP !
```

Now try a simple program to exercise some of these words. Enter:

```
: TYPE-LETTERS 5B 41 DO I EMIT LOOP ;
TYPE-LETTERS
```

to which the machine will respond:

```
: TYPE-LETTERS 5B 41 DO I EMIT LOOP ; OK
TYPE-LETTERS ABCDEFGHIJKLMNOPQRSTUVWXYZOK
```

Now have a look at memory with the DUMP command. Type:

```
0000 80 DUMP
```

and examine the results (remember we put the machine in HEX). Try another WORDS and observe the first word displayed. It has become the word TYPE-LETTERS entered above.

Your NMIS-0021 is now running and communicating as it should.

PARALLEL PORTS

The F68HC11 has five parallel ports, Port A, B, C, D and E. Two ports of the F68HC11 are sacrificed to create an 64K address and data bus. The remaining three ports, A, D and E, are available on the edge of the board. Port A and E are on the right hand side along with VRH and VRL. Port D is on the left hand side of the board. Each of these ports has a row of eight pins to be used for connection purposes. Although some port lines have special multiplexed functions, they can all be used as inputs or as outputs according to their individual designs. Some of the port lines have direction registers allowing them to be used as either inputs or outputs.

The lines can be used as individual inputs or outputs or in combination. There are very few applications, however, where pins are switched dynamically, sometimes used as inputs, sometimes as outputs.

The simplest form of input device is a switch to ground, to create a low level when the switch is closed, with a pull up to give a high level when the switch is open. This switch can be breaker points, reed switch, the contacts of a relay, microswitch, etc. To try an example of this type input, hook up a simple push button switch to Port A Line 0 (PA0) with a 10K ohm pull up resistor to +5.

Push Button Input

The following program will show the current state of the switch.
Enter LOOK to run it.

```
B000 CONSTANT PA
: SWITCH PA C@ 1 AND ;
: CHECK-STATE IF ." OPEN" ELSE ." CLOSED" THEN CR ;
: LOOK SWITCH BEGIN SWITCH 2DUP = IF DROP ELSE SWAP 0=
  CHECK-STATE THEN ?TERMINAL UNTIL ;
LOOK
```

Whenever the switch changes state, open or closed, the computer follows with a written report.

Other possible input devices are shown here.

Input Devices

Note that due to the 10K pull up on the port, the "switch" must sink .5 ma to ground with no more voltage rise than an HC low level (2/10ths of Vcc) at the pin. (A voltage of 7/10 Vcc will always be recognized as a logical one.) Voltages applied above Vdd or below 0 Volts can damage the computer.

The outputs of the F68HC11 can sink 1.6 ma to ground while letting the pin go no higher than 0.4 Volts for a "zero" and source about .8 ma at 4.5 Volts for a "one". In terms of control, this is a very small signal. Most relays require over 50 times more current to operate. LED's typically take 5 ma to be visible. HC levels are such that the output is sufficient to drive the input on one pin of one TTL device or about a dozen of the lower power LSTTL inputs. The output is sufficient to drive VMOS FET's directly, and Darlingtons with an external pull up which can in turn control several amps of current. Usually, however, a buffer will be needed to do serious non-HC interfacing.

Output Devices

To test the output capabilities, wire one of the two circuits shown here or use an oscilloscope or logic probe.

Logic Level Indicators

When the output is a "1" the LED will be on. When the output is a "0" the LED will be off. The following program will exercise the outputs of the 68HC11.

```
: RUN-UP FF B000 C! 0 BEGIN 8 + B000 C! ?TERMINAL UNTIL ;
```

Port A has bits 0,1 and 2 as fixed input and bit 3,4,5 and 6 as fixed output. Bit 7 is bidirectional and can be configured as an output by writing a bit in DDR7 of location B026. Bit 7 is not used in this example. Notice that bit 3 and 4 are changing faster than bits 5 and 6. They are changing so fast that the LED appears to be continuously on at low brightness. Higher numbered Port A lines, bits 5 and 6,toggle at slower rates. Each bit position toggles at 1/2 the speed of the next lower bit.

SERIAL I/O

The F68HC11 has two serial channels, one synchronous and one asynchronous. Both operate at HC levels. The synchronous port is designed for a three wire master/slave clocked channel. There are many peripheral chips designed to work directly with this port, such as A/D and D/A converters, display drivers, etc. The asynchronous port is a full duplex hardware serial channel. To use this serial channel with most standard communications interfaces, level converters are needed.

The NMIS-0021 uses only lines PD0 and PD1 for the asynchronous serial in and serial out respectively, and a ground. Many terminals require additional handshaking signals to work, the NMIS-0021 does not have these signals. In order to fool the terminal, pins 4 and 5 can be hooked together on the DB25F connector, as can pins 6 and 20. In this way the terminals that require the additional handshake signal have their own " clear to send" / "ready to send" and "data terminal ready" / "data set ready" signals wrapped back around, indicating "always ready".

Some systems use software protocols to control serial flow. They generally use the characters ^S to stop and ^Q to continue transmission. This is called the XON/XOFF protocol. The Max-FORTH firmware on the NMIS-0021 does not support this protocol, although it can be added by installing new low level serial routines.

The diagram below is a simple level shifter to allow RS-232 communication between the NMIS-0021 and a video terminal.

Simple Level Shifter

POWER SUPPLY

The main power supply for the NMIS-0021 should be a regulated 5 volt supply. The voltage can be 4.75 to 5.25 volts DC. The NMIS-0021 normally draws less than 50 ma., although the addition of other 2x4"sTM will increase the required current.

The ideal voltage for the VBB supply is 4.3-4.5 Volts. (See the next section for further details.) VBB supplies may work as low as 2.5 Volts. Current requirements are quite small, typically in the 10ua. range. When the VBB supply is used on the processor, it will retain its User Area through power down and remember its linkages to the external FORTH dictionary, etc..

BATTERY BACK UP AND RESET

The battery backup capability will allow data retention in otherwise volatile CMOS RAMs and the processor's own internal RAM through main board power downs. The backup power is supplied temporarily by an on board capacitor or more permanently by a user supplied battery. A terminal has been supplied, marked VBB for Voltage Battery Backup.

The VBB terminal and the backup capacitor are connected to the VBB supply rail on the board by diode, D1. The VBB supply rail supplies the two 28 pin JEDEC sockets, the 8054HN low voltage indicator in the reset circuit, the 74HC00 gate and the 74HC138 decoder. Under normal powered operation, if no power is applied to the VBB terminal, the VBB rail is supplied from the +5 Volt rail through the intrinsic diode of P channel FET, Q1, and the signal diode D2, to within a diode drop of the suppling 5 volt rail (~4.4 Volts). (This may cause some problem with the Dallas Semiconductor DS1223 battery sockets, as they "write protect" their RAMs at 4.75 Volts and are slow to come out of that protection state. This will usually manifest itself as a failure of a program in the battery sockets to autostart on power up. Running an elevated 5 Volt supply may be necessary to accommodate these parts. The purpose of this new feature is, however, to do away with the need for those devices in final system configurations.) When the 8054HN low voltage indicator releases the reset line, Q1 is turned on and the VBB comes almost completely up to the 5 volt rail (~4.95 Volts).

When the 8054HN low voltage indicator holds the reset line low (when VBB is below 3.8-4.2 Volts), Q1 is turned off and the address decoder is disabled through the same input that is used by

MEMDIS. This "access" protects the memories during the power down cycle.

To meet the full letter of the specifications of the parts involved the correct backup voltage on the VBB pin is critical. This supply must be low enough to ensure that after the diode drop of D1, the VBB rail cause the 8054HN to issue a reset (~4.0 Volts), otherwise Q1 will remain on and the whole system will be powered by VBB. It must also be high enough to ensure that after the diode drop of D1, the VBB rail will meet the processors required backup voltage (listed as 4.0 Volts). Therefore, the ideal voltage for the VBB supply is 4.3-4.5 Volts. It should be pointed out however that the Motorola specification appears to be overly conservative. By empirical test, VBB supplies below 3 Volts appear to be quite adequate. Most CMOS RAMs will retain data down to 2.2 Volts. Accounting for the diode drop under such low currents, the VBB supply may work as low as 2.5 Volts. Another consideration is that the 5V supply rail is hooked to the VBB terminal via the D2 diode. There may be a problem if the VBB

supply can not stand the application of ~4.4 volts. Three "AAA" batteries might be an ideal solution as this supplied voltage would tend to keep them charged during powered periods.

The processor battery backup supply enters the chip via the MODB pin. Jumper block B controls the setting of MODB, either to ground or to VBB. For backup of the processor's RAM to be successful jumpers A and B must be in the Single Chip or Expanded Multiplexed settings. When the VBB supply is used on the processor, it will retain its User Area through power down and remember its linkages to the external FORTH dictionary.

When the voltage at the 5v supply rail drops below 3.8-4.2 Volts and no external VBB is supplied, the NMIS-0021 0.1 farad capacitor memory back up system starts a slow discharge.

Depending on the amount of RAM on board and the power efficiency of the individual devices, the capacitor system will back the memory for days. Tests that were performed suggest at least 4 days backup of a single RAM and possibly a week of storage without power can be realized in ideal situations. Use of "mixed" MOS RAM, non CMOS RAM or EPROM in one of the sockets can reduce the backup substantially. Most CMOS EPROMs will not affect the discharge much more than a CMOS RAM. At any rate, this system makes the board resistant data loss during black outs and temporary power failures.

A point to remember with this feature is that a power cycle will not clear a crashed system if the dictionary linkages are blown. Use of a CNTL-G key combination followed by a reset will force a cold reset. Refer to the Max-FORTH User's manual on "After the Crash" for more information.

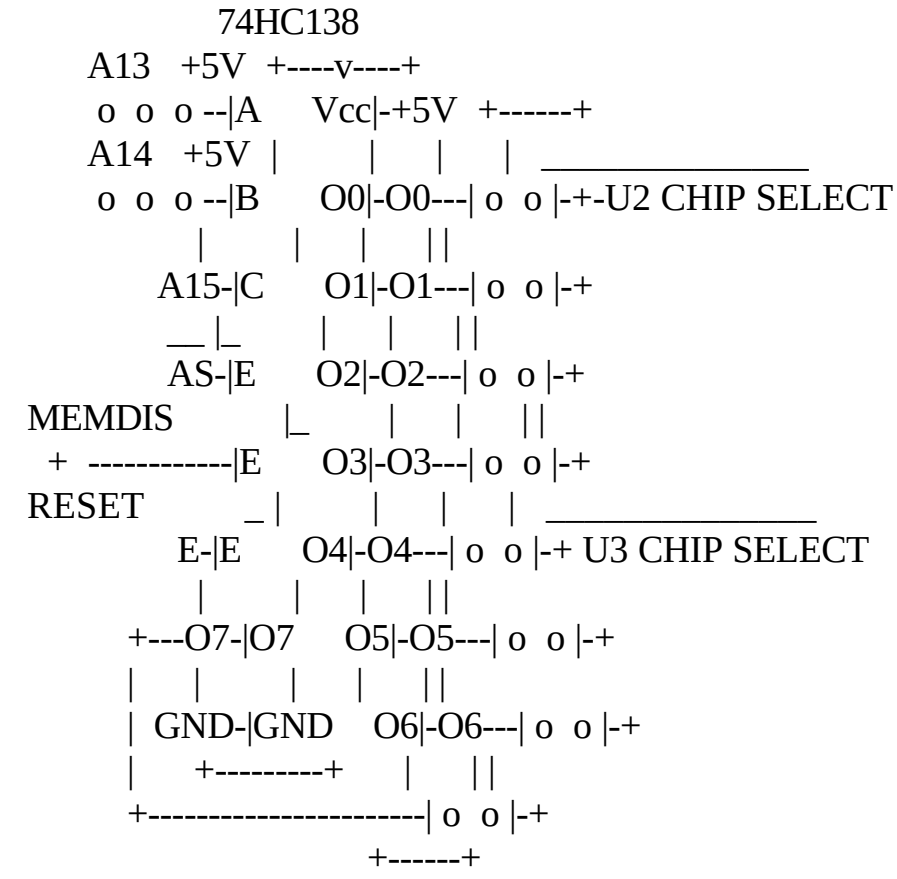
ADDRESS DECODING

The chip selects of the two JEDEC sockets are generated by a 74HC138. When the A13/+5 and A14/+5 jumpers are in the 8K position, address lines A15, A14 and A13 are brought to this part. This means that each of the eight generated chip selects represent a single 8K byte segment out of the 64K byte memory map.

When those jumpers are in the 16K position (not documented on the silkscreen), address lines A15 and A14 are brought to this part. The A13 decoder input is held high. This means that the upper four generated chip selects represent a single 16K byte segment out of the 64K byte memory map.

When they are in the 32K position, address lines A15 alone controls the part. The A14 and A13 decoder inputs are held high. This means that each of the two upper chip selects represent a 32K byte segments out of the 64K byte memory map.

Two other signals control the decoder - Address Strobe (AS) and On Board Memory Disable (MEMDIS). The Address Strobe (AS) signal must be active low before any chip selects are enabled. This is the processor's signal indicating the address on the bus is valid for the off-chip memory. The On Board Memory Disable (MEMDIS) signal allows an offboard open collector source to disable the on board decoder, so offboard components can disable a memory segment from on board memory, even if the entire 64K is filled with RAM on the main board.



Address Decoder

BOARD MOUNTING

The NMIS-0021 has three mounting holes, one in the corner nearest the 34 pin Vertical Stacking Connector which is main the mechanical mounting hole, and two in the opposite corners used for alignment. Each hole is drilled at .110 inches. This will allow passage of a 4-40 screw shaft.

If additional 2x4"sTM are to be used they may be stacked above or below the CPU, as desired, on the female or male side of the Vertical Stacking Connector respectively. A simple hex 3/4 inch standoff with a male screw on one end and a female threaded hole on the other is the ideal interboard connection device. The Vertical Stacking Connector was designed to work with this size spacer, giving reliable board to board connection.

The length of the standard spacer, .750 inches, plus the board thickness, .061 inches, gives a nominal spacing board to board of .811 inches. If an exact spacing of .800 inches is desired (some standard mounting hardware have .800 inch mounting board guides) .011 inches of the mounting surface at the female end of the soft brass standoff can be removed by mill or metal file.

Only the mounting hole near the Vertical Stacking Connector has sufficient clearance around the hole to allow for the head of a screw or the flats of the standoff to rest on. The trace closest to the hole is GND on the top side of the board. All 2x4"sTM are designed with this same convention.

The two mounting holes at the other end board can be used for alignment pins, but do not have sufficient clearance to allow the use of screw. All 2x4"sTM attempt to follow the convention, main-

taining these two mounting holes. If, however, there is sufficient reason to use that board space they may not always be preserved.

The extremely small size of the boards means there are no guaranteed limits on how close components will be placed to the edge of the 2x4"sTM. Board guides will be difficult to use and designs should take this into account. They may be acceptable if non conductive and very shallow. The main mounting hole remains the best point of support.

TROUBLESHOOTING

As always the first thing to do when troubleshooting is to check the power and ground connections. An oscilloscope should be used to check signals. The mounting hole by VRH and VRL is a convenient place to hook a ground clip. If +5 Volts is present at the +5 pin and the board is not operational, the next item to check is the oscillator. Putting the scope on EXTAL (Pin 7) should show a 8 Mhz sine wave (4 Mhz for F68HC11 parts running 4 Mhz XTAL's) running from about .5 Volt lows to 4.5 Volt peaks. XTAL (F68HC11 Pin 8) should have an identical signal, but of a much smaller amplitude. If the sine waves are not present and there is 5V present at the power pin Vcc (Pins 26), and ground at Vss (Pin 52), then either the F68HC11 or the crystal are bad and require replacement. There is one exception. If the processor has executed a STOP instruction, the oscillator will stop. When the oscillator is functioning correctly a 2 Mhz (1 Mhz) clean running square wave should be present at the E output (Pin 5). The E signal drives the timing for all external memory transfers. This signal should toggle nearly rail to rail, a 0.4V low and a 4.6V high are normal. Less amplitude can indicate a board short or an excessive load on the line external to the F68HC11.

The serial channel should send a sign on message if no autostart ROM interferes. If not, the reset circuit could be bad, the serial converter could have failed, or the F68HC11 could be defective. When the RST pin is shorted to ground and released the reset pin (Pin 17) should drop to ground and rise back to 5 Volts in a fraction of a second. If the reset pin is working and still no message is seen on the terminal, check PD1, the serial output line (Pin 33). When reset is exercised, this line should go from normally high through a multitude of toggles back to a high

state. The periods of the toggle transitions are multiples of approximately 100 microseconds. If this signal is not present, and there are no user ROMs in the board, the F68HC11 is suspect. If the signal is present, check pin 3 of the DB25F connector. It should normally be at -V (-5 Volts nominally) and should toggle to +V (+5 Volts nominally) at the same rate as the serial output line (this applies specifically to the circuit in SERIAL I/O or the NMII-0232). If this is happening and no message is seen, the RS-232 wiring or the terminal is suspect. Check to see if the level shifter and NMIS-0021 are connected to the DB25F RS-232 connector as follows:

DB25F	Signal Name
1	Case ground
2	Serial in (to level shifter then to NMIS-0021)
3	Serial out (from level shifter then to NMIS-0021)
7	Electrical ground

DB25F SIGNAL PIN OUT

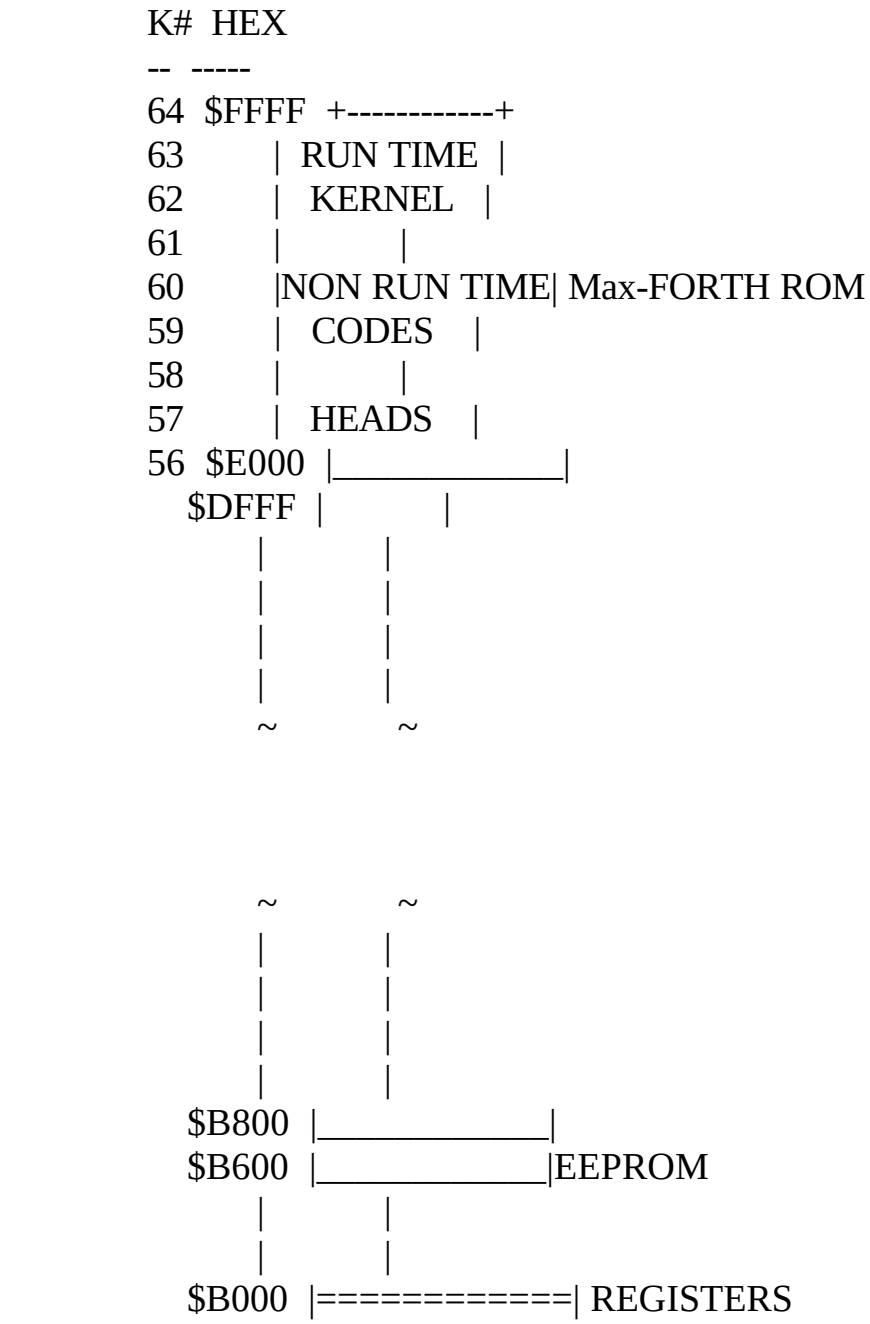
Check the voltages on pins 2 and 3. If pin 3 is very negative and pin 2 is floating, both systems are trying to talk on the same line. Pins 2 and 3 need to be swapped. Usually this is done with a "null modem" inserted where the two systems connect.

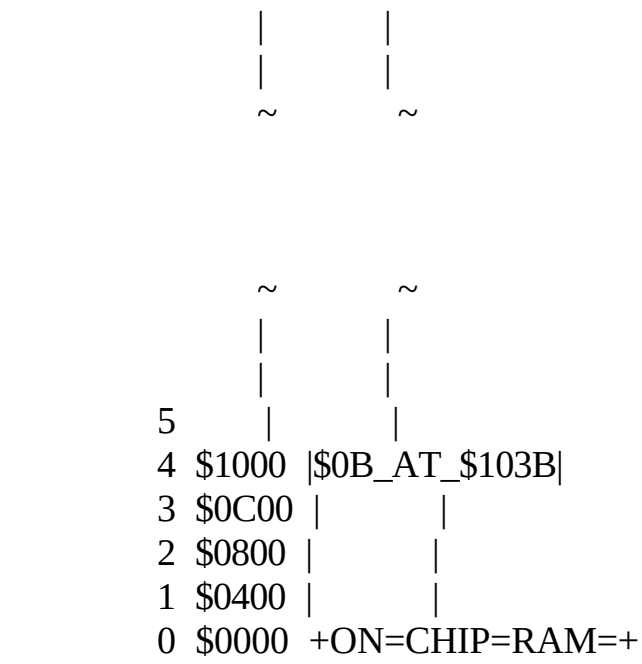
If the -V/+V signal was not found at pin 3, the RS-232 converter is not working. Check the wiring of the RS-232 converter and power and ground on the level shifter.

Check SI which is the serial into the board from the terminal. It should normally be at a +5 Volts. When a key is pressed on the terminal it should pulse to 0 Volts. If it doesn't, the terminal or the RS-232 wiring are suspect. The same signals should also be at PD0, which is the serial input line of the processor (Pin 34).

The most common error in trying to use the NMIS-0021 is mis-matched baud rates or bit settings. Verify that the terminal is set for 9600 baud with one start bit, eight data bits and one stop bits, with no parity generated. (Review this discussion in the Getting Started section.)

MEMORY MAP


K# HEX
-- -----
64 $FFFF +----------+
63 | RUN TIME |
62 | KERNEL |
61 | |
60 |NON RUN TIME| Max-FORTH ROM
59 | CODES |
58 | |
57 | HEADS |
56 $E000 |__________|
$DFFF |
$B800 |__________|
$B600 |__________|EEPROM
$B000 |==========| REGISTERS



Memory Map

VARIOUS JUMPERS

#	SOURCE	DESTINATION	NORMALLY
A13-A	ADDRESS LINE 13	ADDRESS DECODER INPUT	
A-5	+5 VOLT RAIL		
A13-A	ADDRESS LINE 13	ADDRESS DECODER INPUT	
A-5	+5 VOLT RAIL		
O0-U2	DECODER OUTPUT 0	U2 JEDEC SOCKET	
O1-U2	DECODER OUTPUT 1	U2 JEDEC SOCKET	
O2-U2	DECODER OUTPUT 2	U2 JEDEC SOCKET	
O3-U2	DECODER OUTPUT 3	U2 JEDEC SOCKET	
O4-U3	DECODER OUTPUT 4	U3 JEDEC SOCKET	
O5-U3	DECODER OUTPUT 5	U3 JEDEC SOCKET	
O6-U3	DECODER OUTPUT 6	U3 JEDEC SOCKET	
O7-U3	DECODER OUTPUT 7	U3 JEDEC SOCKET	
A			
GND-D	GROUND	MODA PIN	OPEN
D-5	MODA PIN	+5 VOLT RAIL	CLOSED
B			
GND-E	GROUND	MODB PIN	OPEN
E-5	MODB PIN	+5 VOLT RAIL	CLOSED
XIRQ-B	NMI	INT FROM J4	OPEN
B-IRQ	INT FROM J4	PA3 EDGE SENSITIVE LINE	OPEN

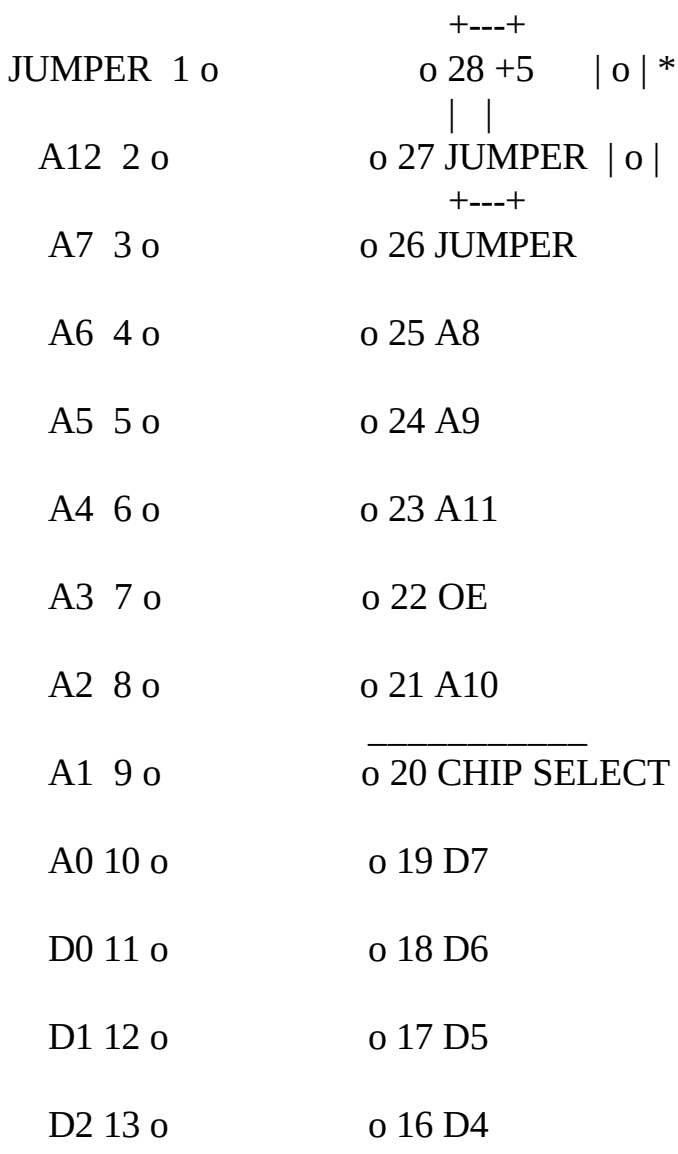
U2	U2 PIN 27 R/W LINE	U2 PIN 28 SUPPLY	OPEN*
U3	U3 PIN 27 R/W LINE	U3 PIN 28 SUPPLY	OPEN*

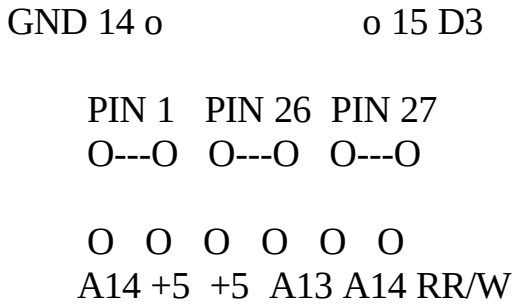
* Optional use of pull-ups on R/W lines can write protect RAMs in socket. To use, install 100K pullup resistor & remove jumper from JEDEC selection pin set for pin 27. If battery backup is in use, RAM will then emulate ROM.

Miscellaneous Jumpers

SOCKET PINOUTS

Jumper Assignments for JEDEC 28 Pin Sockets





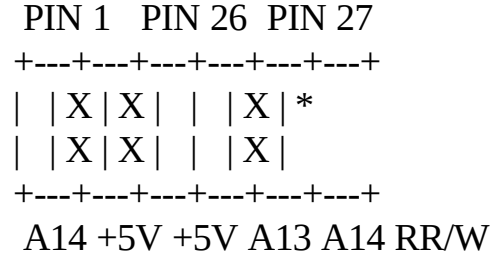
* Optional use of pullups on R/W lines can write protect RAMs in socket. To use, install 100K pullup resistor & remove jumper from JEDEC selection pin set for pin 27. If battery backup is in use, RAM will then emulate ROM.

U2, U3 Socket Pinouts

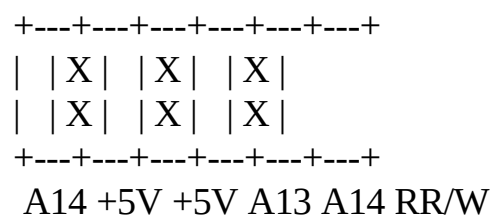
DEVICE SELECTION

Jumper Settings for Standard JEDEC 24/28 Pin Devices

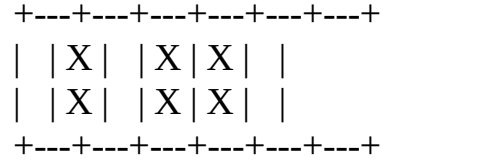
ALL 8K X 8 DEVICES
2764
2864
6264

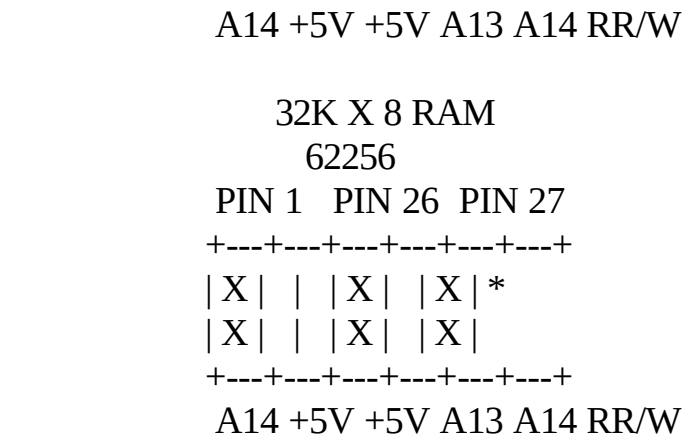


16K X 8 EPROM
27128



32K X 8 EPROM
27256





* Optional use of pullups on R/W lines can write protect RAMs in socket. To use, install 100K pullup resistor & remove jumper from JEDEC selection pin set for pin 27. If battery backup is in use, RAM will then emulate ROM.

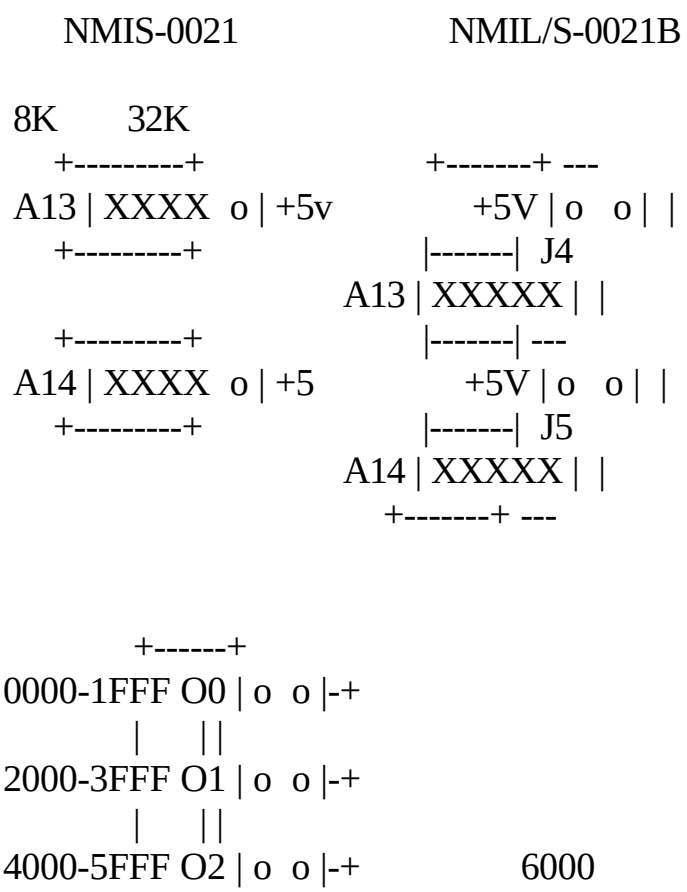
General Purpose Sockets Device Selection

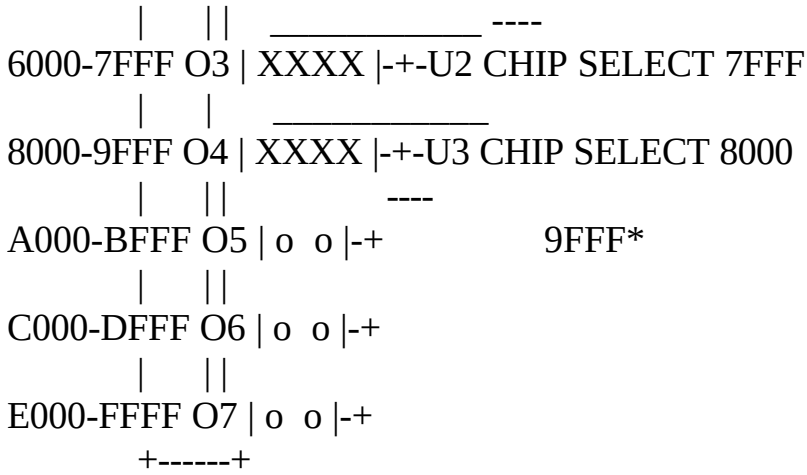
SOCKET ADDRESSING

Jumper Settings for Various Addressing Schemes

(This is one example shown on silkscreen)

2 8K DEVICES





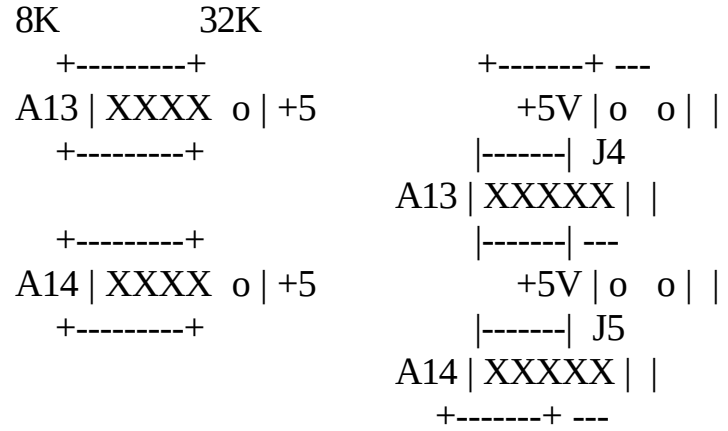
* Note: on the Rev 1.0 & 1.1 silkscreen this is listed as AFFF which is a misprint.

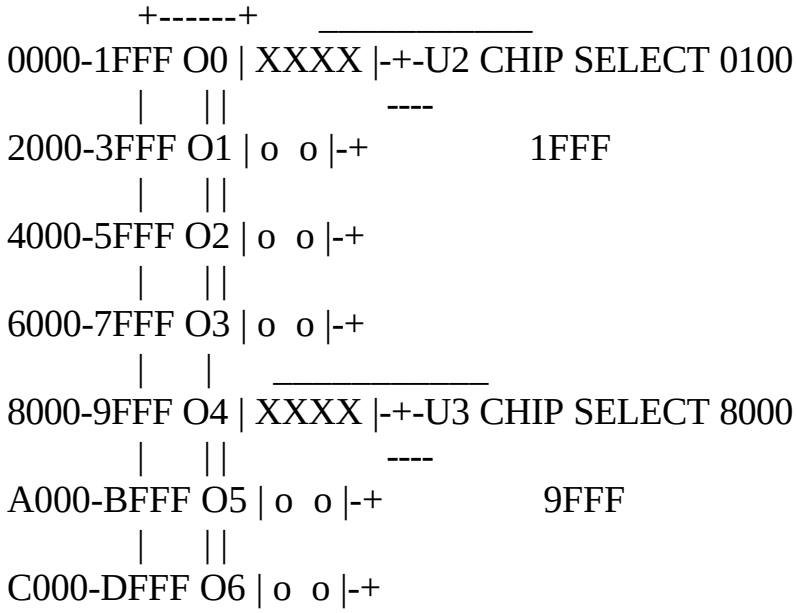
2 8K Devices Contiguous

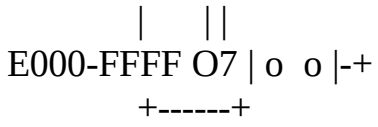
2 8K DEVICES

(This is default factory setting)

NMIS-0021 NMIL/S-0021B



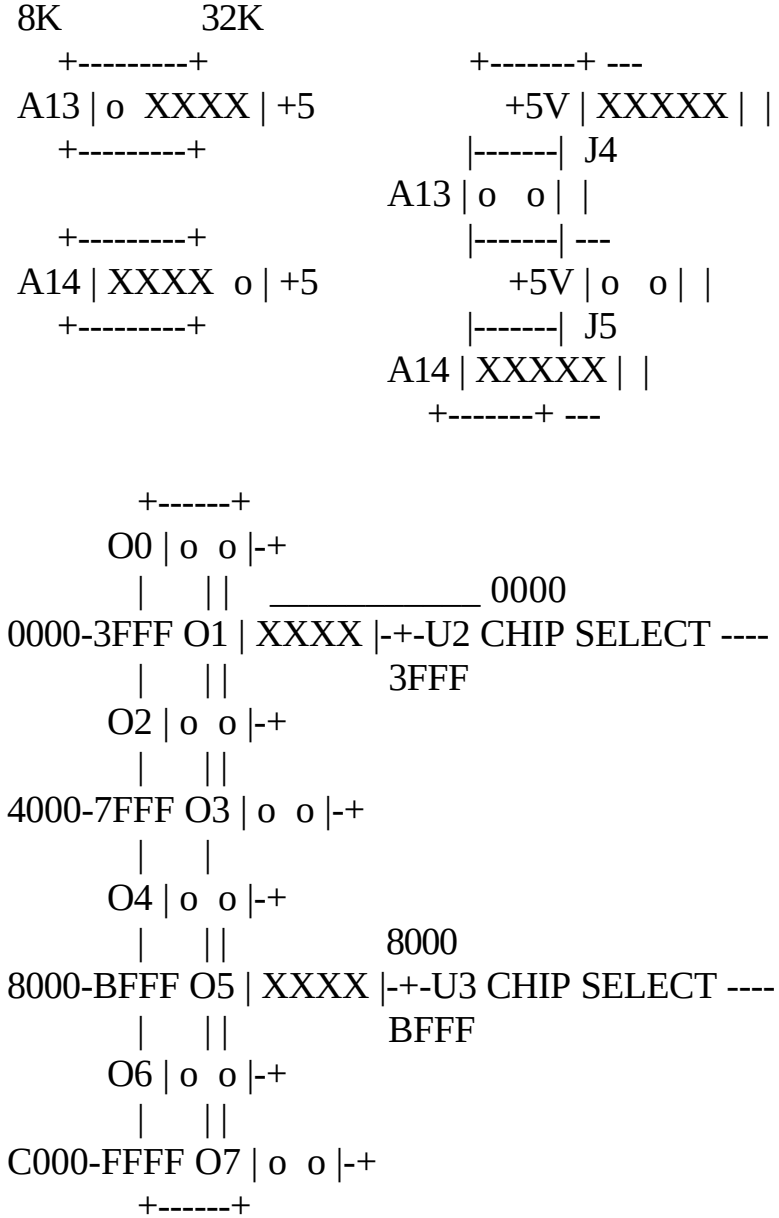




2 8K Devices Default Factory Settings

2 16K DEVICES

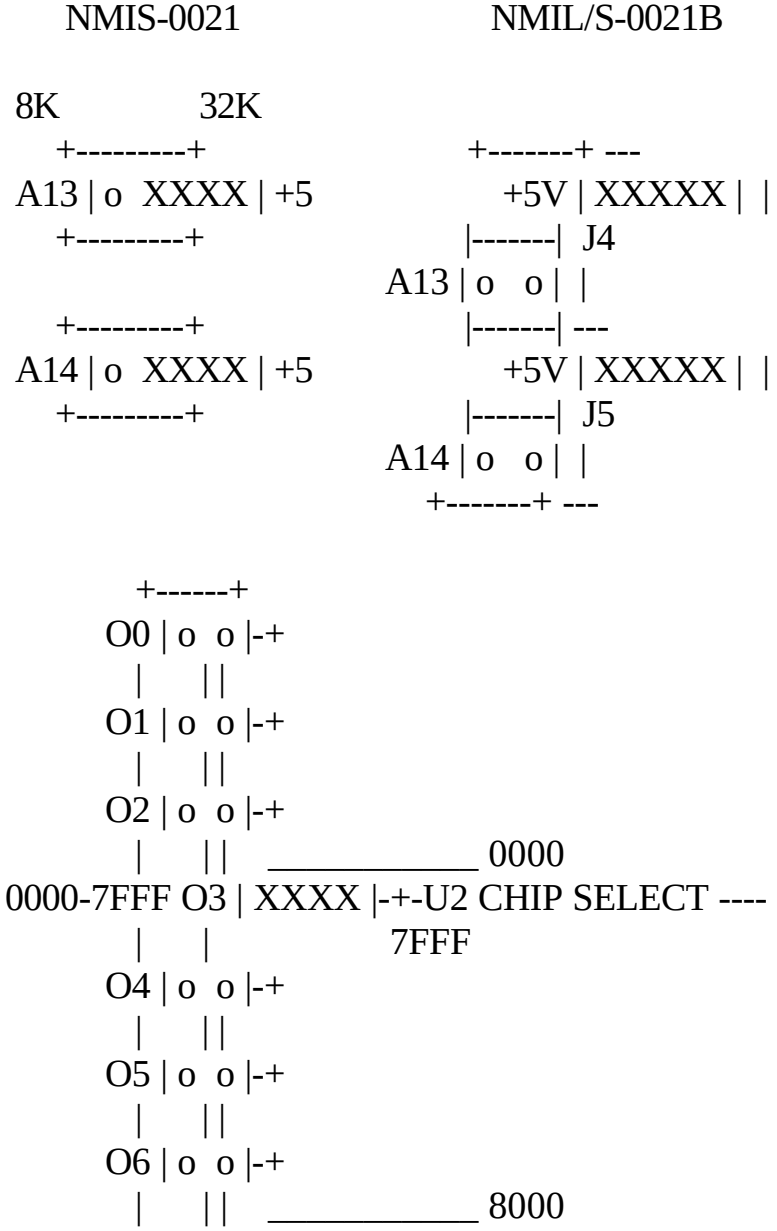
NMIS-0021 NMIL/S-0021B



2 16K Devices

2 32K DEVICES

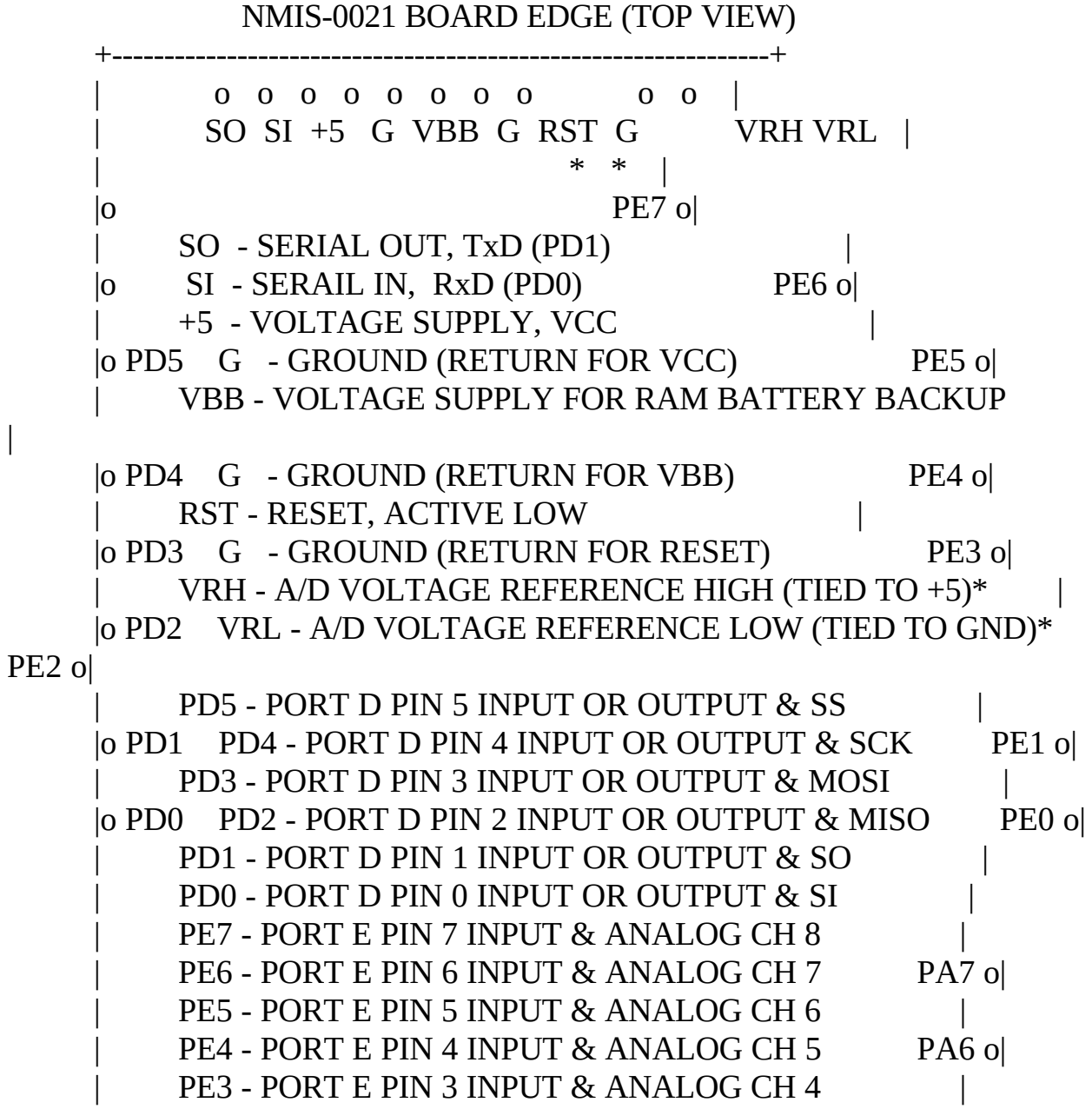
(This is one example shown on silkscreen)

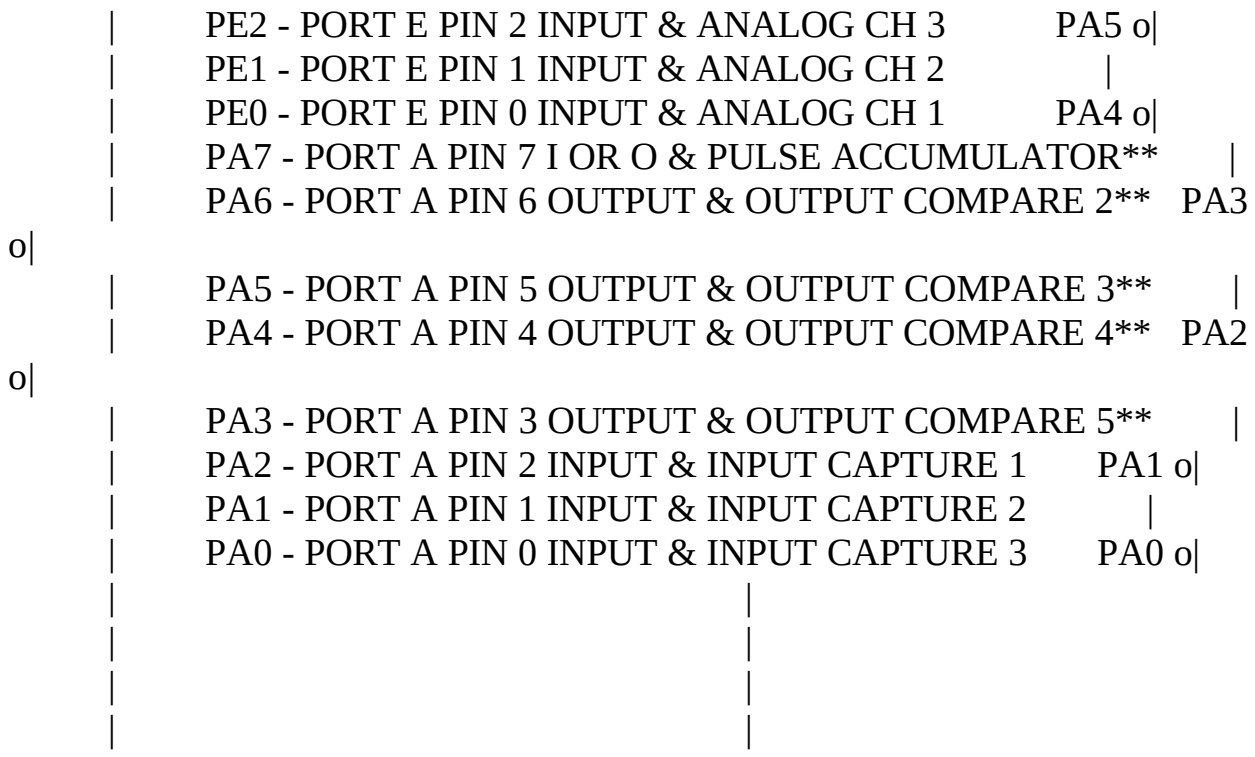


8000-FFFF O7 | XXXX |-+-U3 CHIP SELECT ----
+------+ FFFF

2 32K Devices

CONNECTIONS

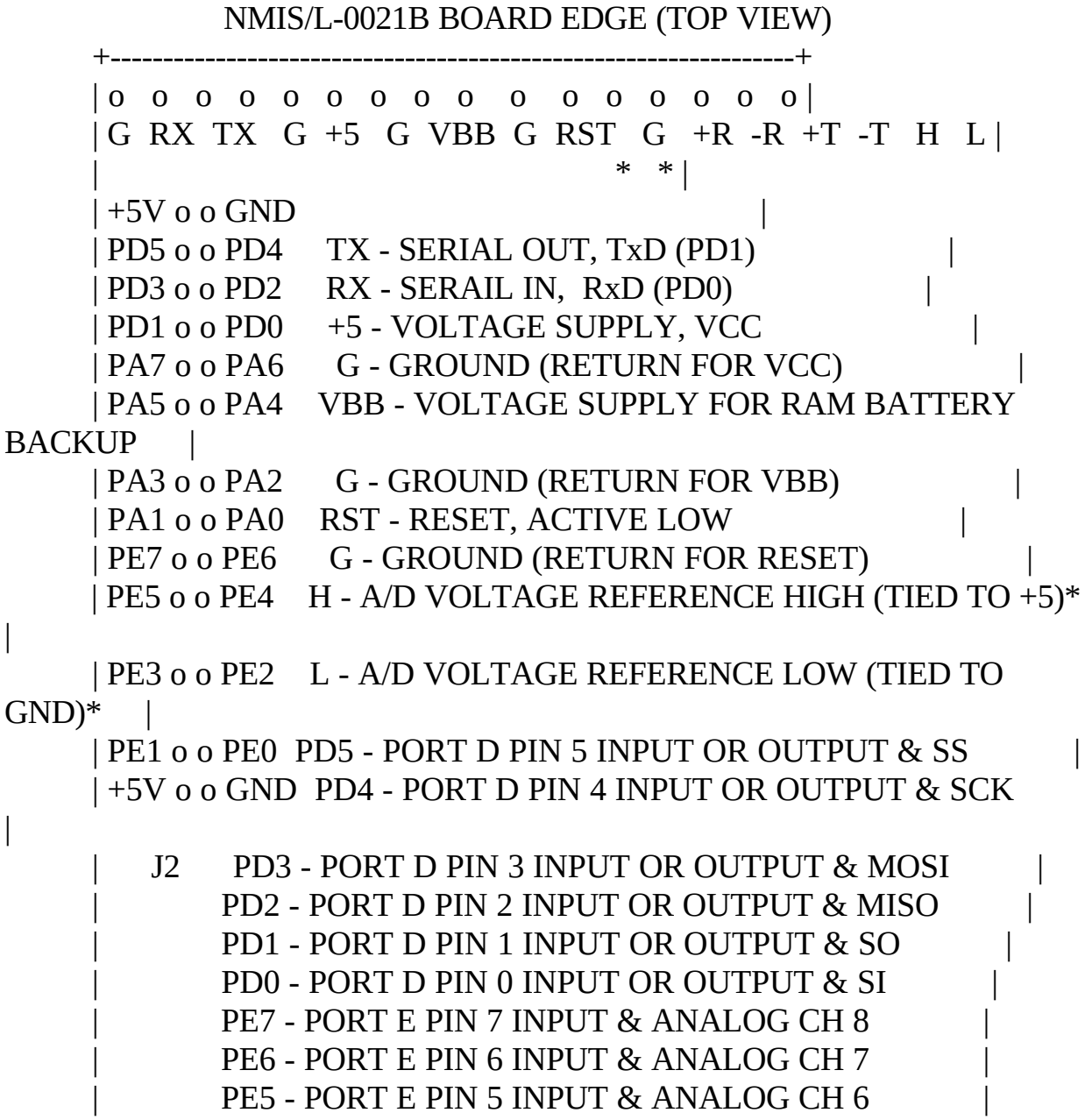




* ATTACHED BY FINE TRACE ON BOTTOM, CUT TO USE REFERENCE SUPPLY

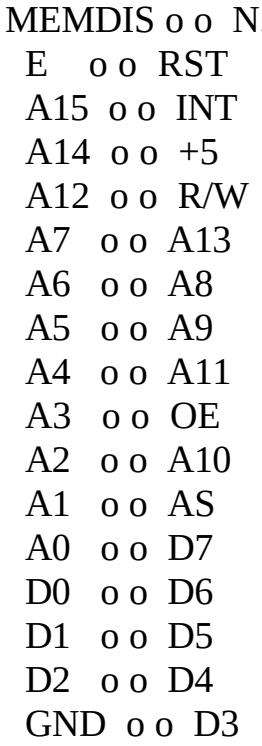
** ALSO OUTPUT COMPARE 1

CONNECTIONS



| PE4 - PORT E PIN 4 INPUT & ANALOG CH 5 |
| PE3 - PORT E PIN 3 INPUT & ANALOG CH 4 |
| PE2 - PORT E PIN 2 INPUT & ANALOG CH 3 |
| PE1 - PORT E PIN 1 INPUT & ANALOG CH 2 |
| PE0 - PORT E PIN 0 INPUT & ANALOG CH 1 |
| PA7 - PORT A PIN 7 I OR O & PULSE ACCUMULATOR** |
| PA6 - PORT A PIN 6 OUTPUT & OUTPUT COMPARE 2** |
| PA5 - PORT A PIN 5 OUTPUT & OUTPUT COMPARE 3** |
| PA4 - PORT A PIN 4 OUTPUT & OUTPUT COMPARE 4** |
| PA3 - PORT A PIN 3 OUTPUT & OUTPUT COMPARE 5** |
| PA2 - PORT A PIN 2 INPUT & INPUT CAPTURE 1 |
| PA1 - PORT A PIN 1 INPUT & INPUT CAPTURE 2 |
| PA0 - PORT A PIN 0 INPUT & INPUT CAPTURE 3 |
| +R - RS-422/485 + DIFFERENTIAL INPUT |
| -R - RS-422/485 - DIFFERENTIAL INPUT |
| +T - RS-422 + DIFFERENTIAL OUTPUT |
| -T - RS-422 - DIFFERENTIAL OUTPUT |

EXPANSION JACK



The Expansion Connector was designed to follow the JEDEC standard for byte sized memory parts in the 8, 16 and 32K Byte varieties. The J4 connector on these boards are made to most closely match the more recently available 32K JEDEC parts.

Expansion Jack (same as J1 of NMIS/L-0021B).

PARTS LIST

NMIS-0021 F68HC11 PARTS LIST REV 1.1

PART#	GENERIC	DESCRIPTION
U1	52 PIN SOCKET	
	F68HC11	FORTH CPU
U2	28 PIN SOCKET	
	2064	8K x 8 RAM
U3	28 PIN SOCKET	
	2064/20256	OPTIONAL MEMORIES U3
U4	74HC00	NAND GATE
U5	74HC138	3 TO 8 DECODER
U6	74HC573	8 BIT LATCH
Y1	8 MHZ XTAL	
J4	34 PIN VSC HEADER	.1" DUAL INLINE
R1	1Meg	1/8 WATT RESISTOR
R2-6	10K	1/8 WATT RESISTOR
C1,2	20 pf	CERAMIC DISC
C3-6	.1uf	MONOLYTHIC BYPASS
C7	.1F	ELECTROLYTIC STORAGE CAPACITOR
LVI1	8054HN	POWER ON RESET MONITOR
Q1	VP0300L	P CHANNEL FET
D1,2	1N4148 OR 1N914	SIGNAL DIODE
PCB	NMIS-0021 PCB	REV 1.0
	JUMPER PINS	BERG STYLE .1" CENTER JUMPERS
	JUMPER SHUNTS	BERG STYLE .1" CENTER SHUNTS

SILKSCREEN

NMIS-0022 Rev 1.1 Silkscreen

MECHANICALS

SCHEMATIC

NMIS-0022 Rev 1.1 Schematic