

NMIS-9002 3CH 16BIT COUNTER CARD

The NMIS-9002, in 2x4" sTM format, provides a JEDSTACKTM computer system with access to three channels of 16-bit counters.

FEATURES

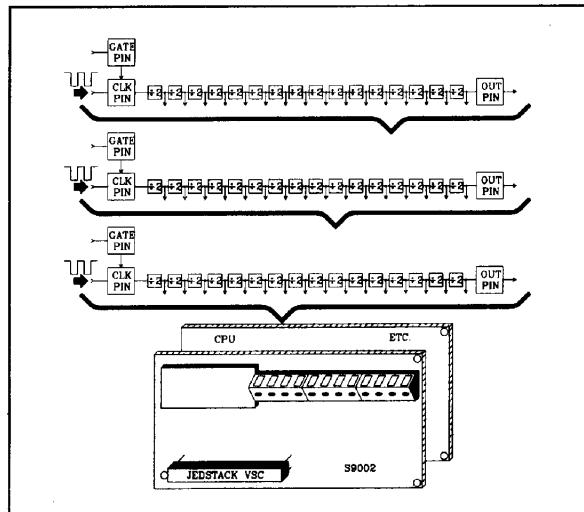
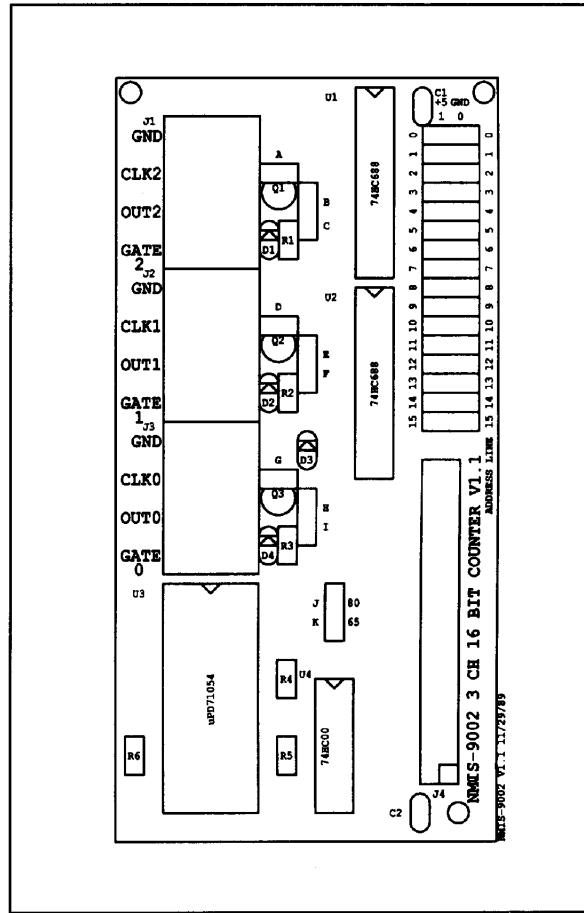
- uPD71054 CMOS counter chip with:
- Three independent 16-bit counters
- Six programmable counter modes
- Binary or BCD counting
- Multiple latch command
- Wide clock rate from DC to 8 MHz
- Low-power standby mode
- CMOS technology

The uPD71054 is a high-performance, programmable counter for system timing control. Three 16-bit counters, each with its own clock input, gate input, and OUT pin, can be clocked from DC to 8 MHz. Under software control, the uPD71054 can generate accurate time delays.

The uPD71054 contains three counters capable of binary, or BCD, operation. There are six programmable count modes. The counters operate independently and each can be set to a different mode.

After initialization, the uPD71054 can count the delay, and generates an interrupt when the task is complete, without further CPU intervention. This eliminates the need for software timing loops and frees the CPU for other tasks.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the drivers' space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-9002 occupies 4 address locations. Any 4-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.



Application

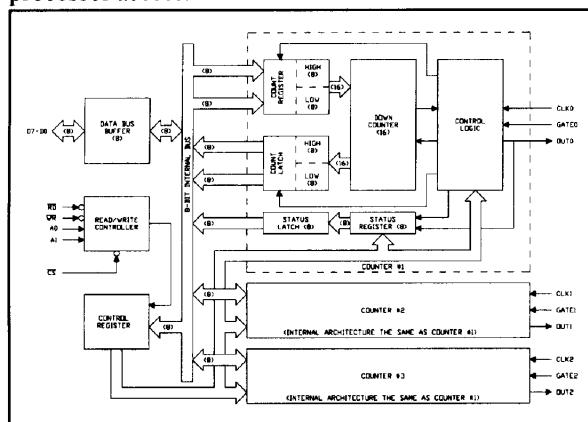
NMIS-9002 3-CH 16-BIT COUNTER CARD 2x4"s

NMIS-9002 3-CH 16-BIT COUNTER CARD 2x4"'

DESCRIPTION

Internally the three counter channels consist of a number of registers. The Command Register is an 8-bit register which is written with the control command determining the operating mode of the counter. The contents of this register cannot be read directly. (The multiple latch command, however, allows you to read the mode and status of each counter.) Binary or BCD operation can be selected, as well as the Count Mode (0-5), the Read/Write Mode, and the counter or counters involved.

Internally the three counters each have three 16-bit registers: the Counter itself, the Count Register, and the Count Latch. The Counter is a 16-bit down counter. The 16-bit Count Register can preset the 16-bit Counter by transferring the desired value to it. The 16-bit Count Latch can capture the Counter, and hold the data for processor access.



Block Diagram

ADDRESS	Read Target	Write Target
XXX0	Counter 0	Counter 0
XXX1	Counter 1	Counter 1
XXX2	Counter 2	Counter 2
XXX3		Command Register

Register Summary

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RWM1	RWM0	CM2	CM1	CM0	BCD

Command Register

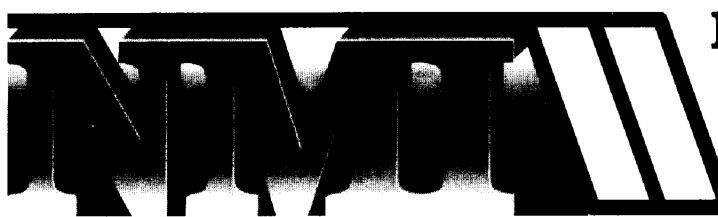
BCD	Binary or BCD		
0	Binary Count (16 Bits)		
1	BCD Count (4 Digits)		
CM2	CM1	CM0	Count Mode
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	0	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5
RMW1	RMW0		Read/Write Mode
0	0		Count Latch Command (2)
0	1		Lower Byte Only
1	0		Higher Byte Only
1	1		Lower Byte, then Higher Byte
SC1	SC0		Select Counter or Multiple Latch Command
0	0		Counter #0 (1)
0	1		Counter #1 (2)
1	0		Counter #2 (3)
1	1		Multiple Latch Command (2)

Command Register Detailed Summary

WORLD HEADQUARTERS

WORLDWIDE REPRESENTATIVES

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