

# NMIS-5008 OCTAL UART CARD

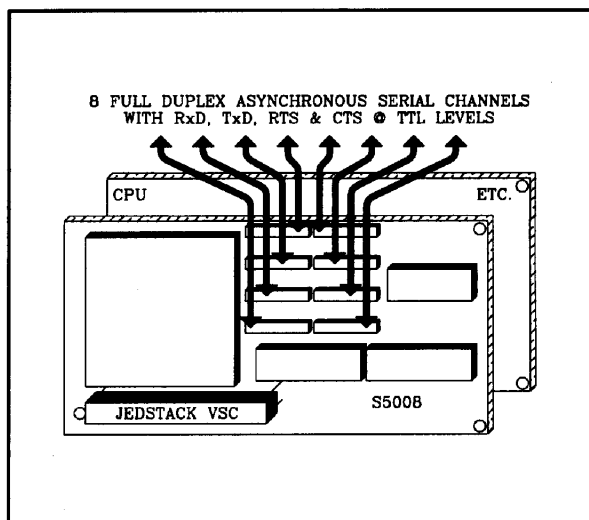
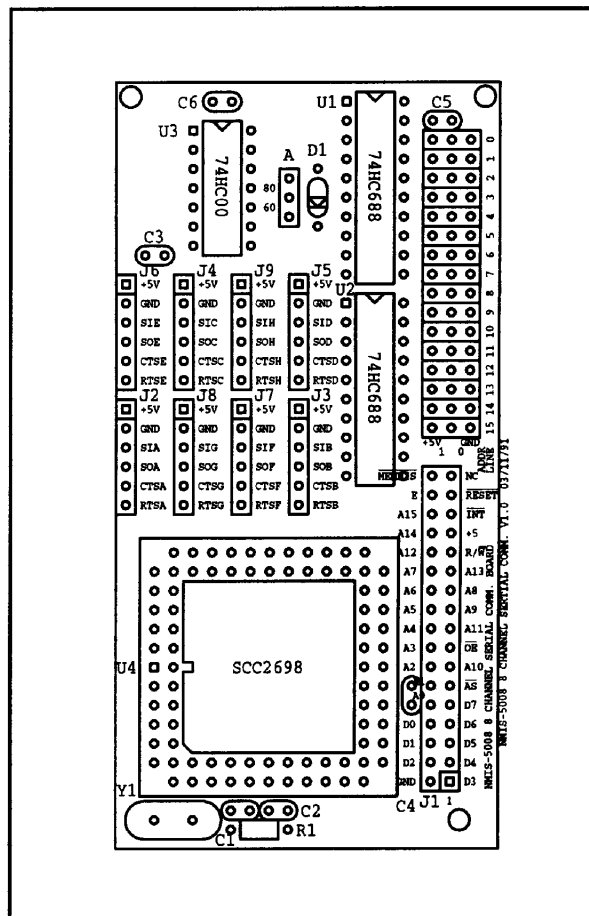
The NMIS-5008 Octal UART Card, in 2x4"s™ format, provides a JEDSTACK™ computer system with eight, full-duplex, Universal Asynchronous Receiver/Transmitter (UART) channels at TTL levels.

## FEATURES

- Eight asynchronous receiver/transmitters
- Quadruple buffered receiver data register
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Baud rate selectable from: 18 fixed rates 50 to 38.4, or, four user-defined rates derived from the programmable counter/timer associated with each of the four blocks, or, External 1X or 16X clock
- Parity, framing, and overrun error detection
- False start bit detection
- Line break detection and generation
- Programmable channel mode: Normal (full-duplex), or, automatic echo, or, local loopback, or, remote loopback
- Four multi-function programmable 16-bit counter/timers
- Eight maskable interrupt conditions
- Programmable edge detect for RTS, and CTS

Each of the channels has a 6-pin, in-line, male header that accepts a cable used on NMI's level shifter boards. The Octal UART chip, a Signetics SCC2698, is the key part on the board. It generates the outgoing serial data and translates the incoming data in processor readable form.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the Octal UART's space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-5008 occupies 64 addresses. Any 64-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.



## Application

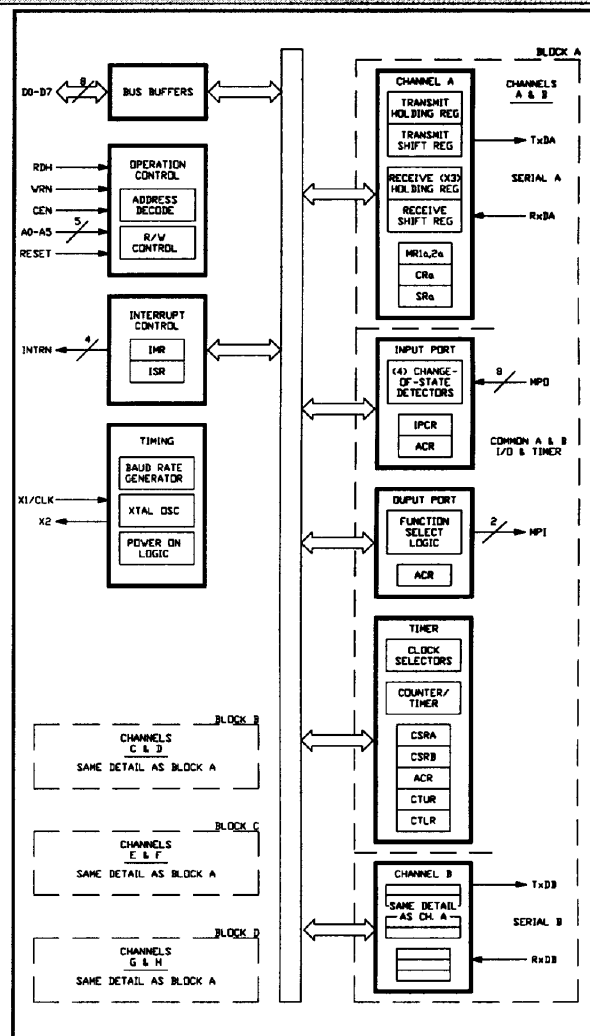
## DESCRIPTION

The Octal UART has an internal baud rate generator. The transmitter baud rate is programmable to any one of 18 different rates from 50 to 38,400 baud. The Octal UART is programmable for word lengths of 5,6,7 or 8 bits; even, odd, forced, or no parity; and 1, 1.5 or 2 stop bits.

The card's serial channels are at TTL levels. Level shifting is not provided. The interface level desired can be set by external level shifters, allowing any mix of RS-232, RS-422, RS-485 and TTL to be selected with this card. Three such cards are designed to perform this level shifting task. The NMII-0232 is designed to provide TTL to RS-232 conversion, the NMII-0422 for TTL to RS-422 conversion, and the NMII-0485 for RS-485.

| BLOCK BASE ADDRESS OFFSET |    |    |    | READ<br>x=A,C,E or G | WRITE<br>y=B,D,F or H |
|---------------------------|----|----|----|----------------------|-----------------------|
| A                         | B  | C  | D  |                      |                       |
| 0                         | 10 | 20 | 30 | MR1x, MR2x           | MR1x, MR2x            |
| 1                         | 11 | 21 | 31 | SRx                  | CSRx                  |
| 2                         | 12 | 22 | 32 | Reserved             | CRx                   |
| 3                         | 13 | 23 | 33 | RHRx                 | THRy                  |
| 4                         | 14 | 24 | 34 | IPCR                 | ACR                   |
| 5                         | 15 | 25 | 35 | ISR                  | IMR                   |
| 6                         | 16 | 26 | 36 | CTU                  | CTUR                  |
| 7                         | 17 | 27 | 37 | CTL                  | CTLR                  |
| 8                         | 18 | 28 | 38 | MR1y,MR2y            | MR1y,MR2y             |
| 9                         | 19 | 29 | 39 | SRy                  | CSRy                  |
| A                         | 1A | 2A | 3A | Reserved             | CRy                   |
| B                         | 1B | 2B | 3B | RHRy                 | THRy                  |
| C                         | 1C | 2C | 3C | Reserved             | Reserved              |
| D                         | 1D | 2D | 3D | Input Port           | OPCR                  |
| E                         | 1E | 2E | 3E | Start C/T            | Reserved              |
| F                         | 1F | 2F | 3F | Stop C/T             | Reserved              |

Register Summary

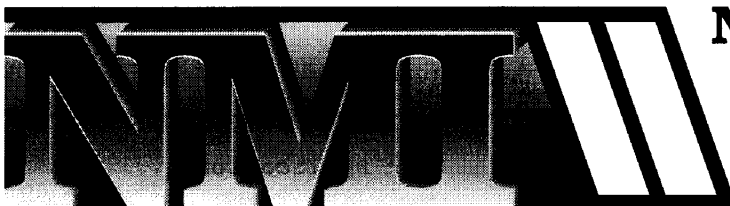


Block Diagram

## WORLD HEADQUARTERS

## WORLDWIDE REPRESENTATIVES

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|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
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