



NMIS-5002 DUAL ACIA CARD

The NMIS-5002 Dual ACIA Card, in 2x4"™ format, provides a JEDSTACK™ computer system with two Asynchronous Serial Channels, at full RS-232C/V.28 levels.

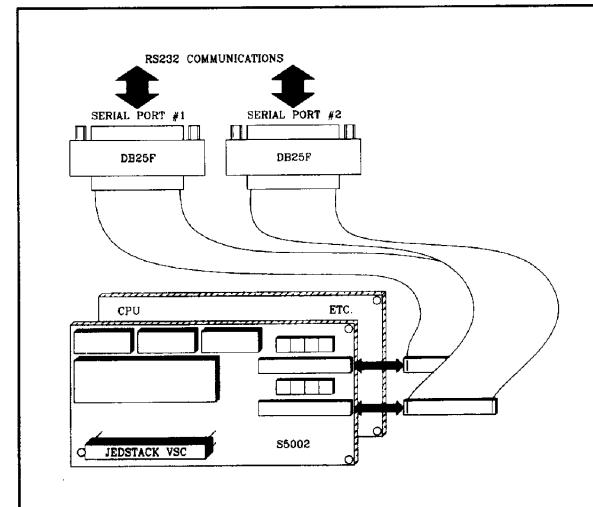
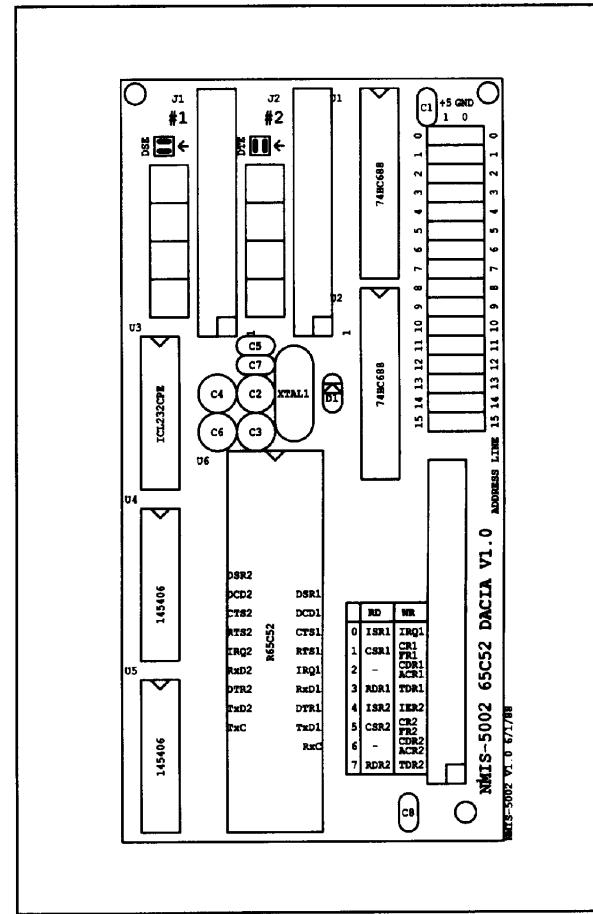
FEATURES

- Two independent, full-duplex RS-232 channels with buffered receivers and transmitters
- Data set/modem control functions
- Baud rate generator with 15 programmable baud rates (50 to 38,400)
- Programmable word lengths, number of stop bits, and parity bit generation and detection
- Programmable interrupt control
- Programmable control of edge detect for DCD, DSR, DTR, RTS, and CTS
- Automatic Address Recognition Mode for multi-drop operation

Each of the channels has a 26-pin, IDC style, male header that accepts a common cable, with a 26-pin female IDC and a DB-25, to connect the board to other communications equipment. This cable was chosen because of its widespread availability. Jumpers are provided to allow the choice of selecting Data Terminal (DTE) or Data Set Equipment (DSE) configurations. This eliminates the need for an additional null-modem.

The Dual ACIA chip, a Rockwell 65C52, is the key part on the board. It generates the outgoing serial data and translates the incoming data in processor readable form. The ACIA channels can be interrupt driven to allow minimum processor overhead.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the Dual ACIA chip's space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-5002 occupies 8 addresses. Any 8-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.

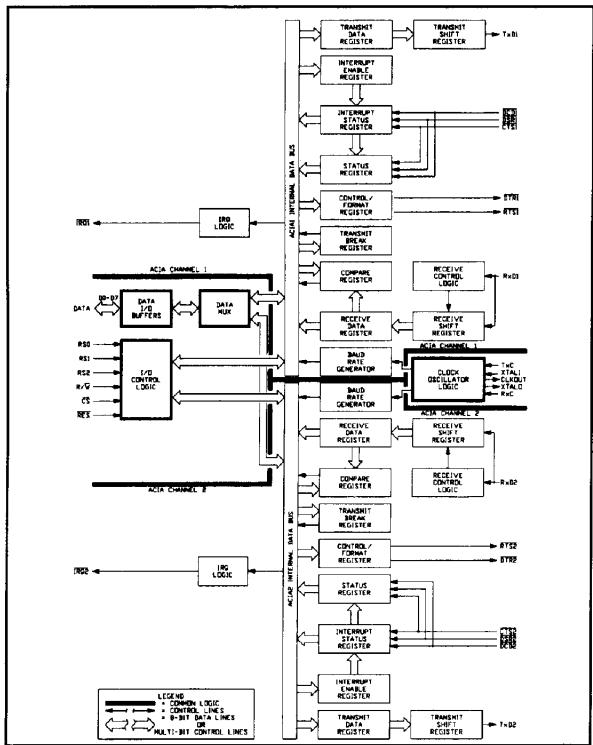


Application

NMIS-5002**DUAL ACIA CARD****2x4"™****NMIS-5002**

DESCRIPTION

The DACIA has an internal baud rate generator. The transmitter baud rate is programmable to any one of 15 different rates from 50 to 38,400 baud. The DACIA is programmable for word lengths of 5,6,7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

**Block Diagram**

The RS-232 level shifting is provided by three chips. The ICL232CPE is a charge pump producing the elevated +9V and -9V needed for RS-232 communications from a single +5V supply. It also contains two pairs of RS-232 line drivers. The MC145406's each contain an additional three pairs of line drivers. These chips convert the CMOS serial data lines to RS-232 levels.

ADDR	CONTROL & FORMAT REG. BITS	REG ABBR	REG ACCESS	
			WRITE	READ
XXX0	-	IER1 ISR1	INTERRUPT ENABLE REGISTER 1	INTERRUPT STATUS REGISTER 1
XXX1	0	CFR1 SR1	CONTROL REGISTER 1	STATUS REGISTER 1
	1	CFR1	FORMAT REGISTER 1	INVALID
XXX2	-	CDR1	COMPARE DATA REGISTER 1	INVALID
	1	TBR1	TRANSMIT BREAK REGISTER 1	INVALID
XXX3	-	TDR1 RDR1	TRANSMIT DATA REGISTER 1	RECEIVE DATA REGISTER 1
XXX4	-	IER2 ISR2	INTERRUPT ENABLE REGISTER 2	INTERRUPT STATUS REGISTER 2
XXX5	0	CFR2 SR2	CONTROL REGISTER 2	STATUS REGISTER 2
	1	CFR2	FORMAT REGISTER 2	INVALID
XXX6	-	CDR2	COMPARE DATA REGISTER 2	INVALID
	1	TBR2	TRANSMIT BREAK REGISTER 2	INVALID
XXX7	-	TDR2 RDR2	TRANSMIT DATA REGISTER 2	RECEIVE DATA REGISTER 2

Register Summary**WORLD HEADQUARTERS****WORLDWIDE REPRESENTATIVES**

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