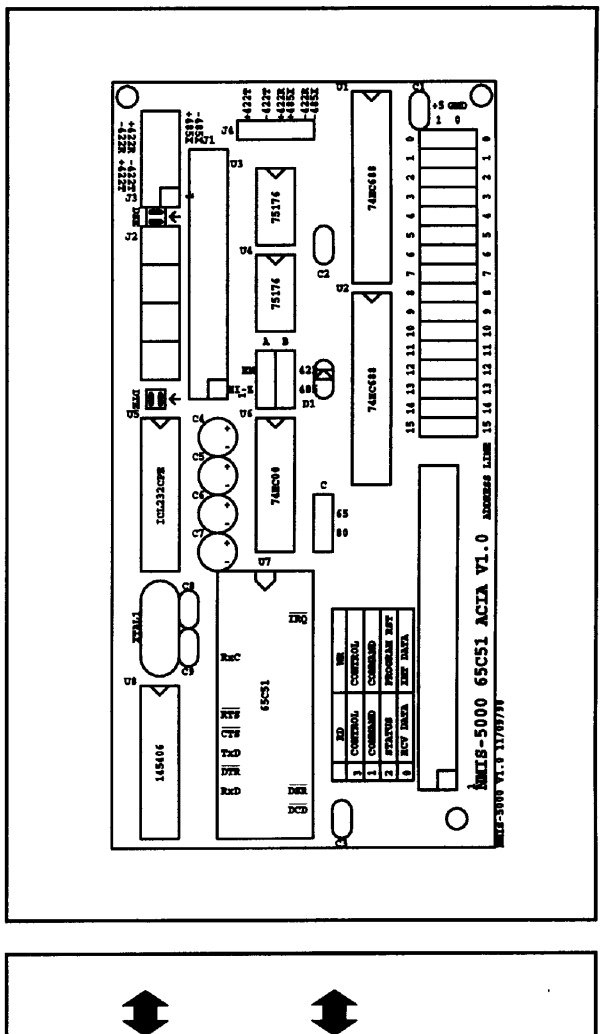
NMIS-5000 ACIA CARD

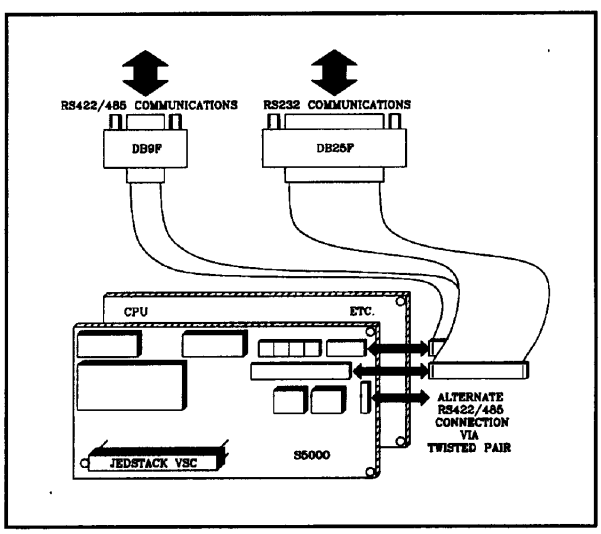
The NMIS-5000 Asynchronous Communications Interface Adapter (ACIA) Card, in 2x4"s™ format, provides a JEDSTACK™ computer system with an industry standard asynchronous serial data transmission capability (RS-232C, RS-422, modified RS-422, or RS-485).



- Full duplex RS-232, RS-422, modified RS-422, or RS-485 operation with buffered receiver and transmitter
- Data set/modem control functions (DTR, DSR, RTS, CTS, DCD)
- Internal baud rate generator with 15 programmable baud rates (50 to 19,200)
- Programmable word lengths, number of stop bits, parity bit generation and detection
- Programmable interrupt control
- Program reset
- Charge pump for +9V/-9V supplies
- Jumper selectable DTE or DSE configuration

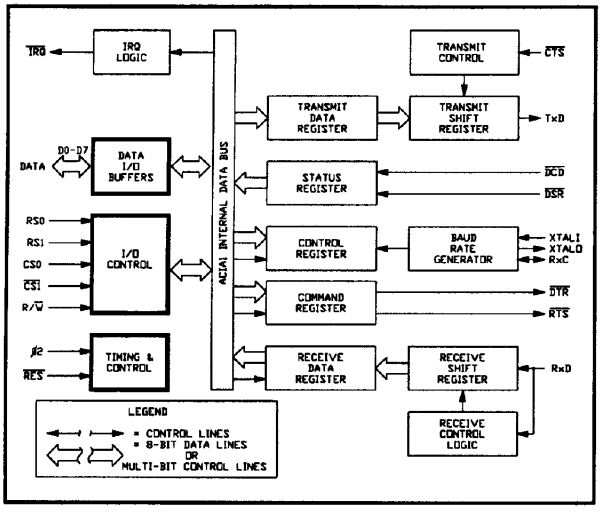
The programmable 65C51 Asynchronous Communications Interface Adapter (ACIA) device is memory mapped into the systems memory by the card. J1 and J2 provide the RS-232 cable connection and configuration. J1 is an IDC, 26-pin cable connector, designed to accept a flat ribbon cable. The J2 connector is really not a connector at all, as such, but a jumper field to direct the correct signals to the connected equipment. Connector J3 is used for RS-422/485 signals. Only one standard, RS-232, RS422, or RS-485 can be selected at a time.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the ACIA chip's space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-5000 occupies 4 addresses. Any 4-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.



The ACIA has an internal baud rate generator. The crystal determines the baud rates. It should be a 1.8432 MHz, series-resonant crystal for a normal selection of baud rates up to 19,200 baud. (Other values may be substituted to get "off" baud rates.) The ACIA is programmable for word lengths of 5,6,7 or 8 bits; even, odd, or no parity; and 1 or 2 stop bits.

The RS-232 level shifting is provided by two chips. The ICL232CPE is a charge pump producing the elevated +9V and -9V needed for RS-232 communications from a single +5V supply. It also contains two pairs of RS-232 line drivers. The MC145406 contains an additional three pair of line drivers each. These chips convert the CMOS serial data lines to RS-232 levels. The RS-422/RS-485 interface signals are received and translated by two 75176's.



The IRQ' output is hooked directly to the interrupt INT' line on the VSC. The ACIA can provide real time interrupts to the processor with this signal as conditions occur that require processor intervention, such as receive buffer full, or transmit buffer empty. It is an "open collector" output that pulls down the pull up on the processor board.

The RES' signal of the 65C51 is hooked to the RESET' line in the VSC. The low voltage detector on the processor should give a power up hardware reset to start the ACIA in a known state. Also the 65C51's R/W input is hooked to the R/W line.

The two receiver systems of the RS-232 and RS-422/RS-485 are wire OR'ed together, and while they will operate in this manner, they are fighting each others' output drivers. Both drivers will try to get their received information to the 65C51. The low signal usually wins the contest. A high signal is the normal "no-connect" condition. (It is recommended that U4 be removed when not needed to avoid this condition.)

ADDRESS	READ	WRITE
XXX0	TRANSMIT DATA REGISTER	RECEIVE DATA REGISTER
XXX1	(PROGRAMMED RESET)	STATUS REGISTER
XXX2	COMMAND REGISTER	COMMAND REGISTER
XXX3	CONTROL REGISTER	CONTROL REGISTER

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