NMIS-3004 64-BIT OUTPUT CARD

The NMIS-3004 64-Bit Output Card, in 2x4"s™ format, provides a JEDSTACK™ computer system with 64 bits of latched outputs. The outputs are arranged to easily connect (by two 34-conductor ribbon cables or by individual wire) to 64 output points, power, and ground.

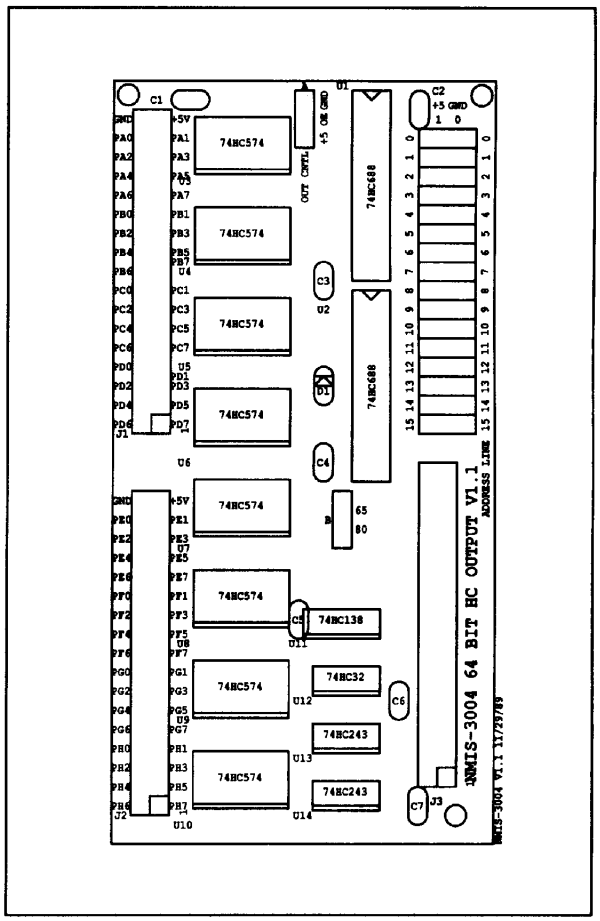
FEATURES

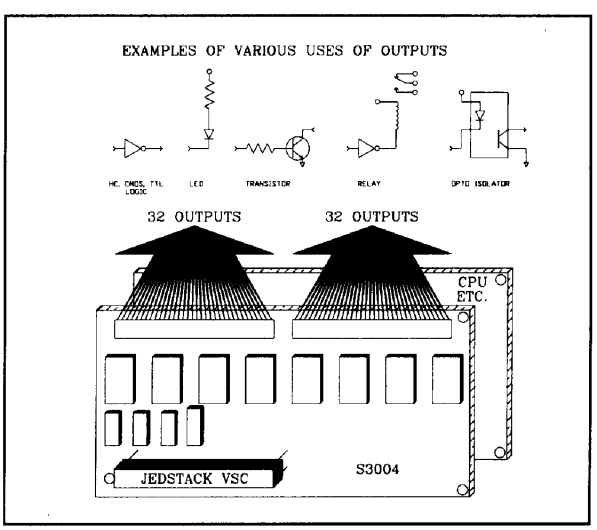
- Eight 8-bit parallel output ports
- Low power HCMOS design
- High current drive: nominal 25 mA. per pin
- Compact size
- Easy connection
- Easy computer interfacing

All the pins of the 34-pin connectors, J1 and J2, can attach to individual output points, except for Pin 33, which is attached to +5V power, and Pin 34, which is attached to system ground. Two 4-bit, bidirectional transceivers buffer the data bus from the loads of the latches. Control logic is used to generate the chip select and timing information to operate the latches and drivers.

The drivers on the latches are controllable by the signal from a provided jumper. When it is set to ground, the drivers on the latches are enabled. The drivers of the latches will control the level on the output pins (providing there is no contention from attached equipment). When it is set to +5V, the drivers on the latches are disabled and the output pins are controlled by external devices. The jumper can be removed, and this input driven by external circuitry. This allows the output drive capability to be selectively controlled by another signal.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the latches' space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-3004 occupies 8 addresses. Any 8-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.





Application

NMIS-3004

NMIS-3004 64-BIT OUTPUT CARD 2x4"s

DESCRIPTION

The NMIS-3004 64-Bit Output Card is designed to stack on the 2x4"s™ NMIS Series, the "100 Squared"™ NMIX, and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The JEDSTACK™ provides interface signals to the board including address lines, data lines, control lines and 5V power and ground. The fast HC devices allow access times approaching 90nS.

The addressing of the octal latches on the NMIS-3004 is sensed by two 74HC688 (U1 and U2) octal comparators that decode the 16 address lines (A15 - A3) and one control line in order to select only four active locations out of a 64K address space.

The 74HC138 uses this signal for one of its negative enables. It also uses Jumper "B" for its one positive enable. Jumper "B" provides a constant high, if set for "80" type processors; or the "E" clock, if set for 6500 and 6800 type processors.The address inputs to the 74HC138 include three address lines (A0, A1 and A2), and the R/W line. The eight decoded chip selects go to the 74HC574 output latches.

The 74HC574's are connected to the Data Bus by way of the 74HC243's. The 74HC243's act as bus buffers, limiting the load placed on the Data Bus to only one HC load (rather than eight). This increases the number of boards that could otherwise be put on the system, due to fan out limitations. By way of these bus drivers, the 74HC574's accept data from the processor. The drivers on the 74HC574's are controlled by the signal from Jumper "A": when set to ground, the drivers are enabled, when set to +5V, the drivers are disabled and the output pins are not controlled.

Output drive capability of the 74HC574 has a sink and source current of 25 mA., at normal 5V operation. Worst case minimums at 25 degrees C, with a 4.5V supply, show a sink current capability of 17 mA., at an output voltage of 1.5V; and a source capability of 15 mA., at an output voltage of 3.0V. The outputs have voltages of 0.1V and VCC-0.1V for an output current of 20 uA., or the equivalent of 20 HC loads. The output drives for standard drive devices are such that they can drive ten LSTTL loads, at full specification, across the full temperature range. The output short circuit currents of these devices will typically exceed the 25 mA. limits. The outputs can be shorted for brief periods of time for logic testing, if the maximum package power dissipation of 500 mW is not violated.

ADDRESS	LATCH	BITS
XXX0	1 U3	1-8 PA0-PA7
XXX1	2 U4	9-16 PB0-PB7
XXX2	3 U5	17-24 PC0-PC7
XXX3	4 U6	25-32 PD0-PD7
XXX4	5 U7	33-40 PE0-PE7
XXX5	6 U8	41-48 PF0-PF7
XXX6	7 U9	49-56 PG0-PG7
XXX7	8 U10	57-64 PH0-PH7

Register Summary

WORLD HEADQUARTERS WORLDWIDE REPRESENTATIVES

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