NMIS-3003 64-BIT INPUT CARD

The NMIS-3003 64-Bit Input Card, in 2x4"s™ format, provides a JEDSTACK™ computer system with 64 bits of latchable inputs. The inputs are arranged to easily connect (by two 34-conductor ribbon cables or by individual wires) to 64 input points, power, and ground.

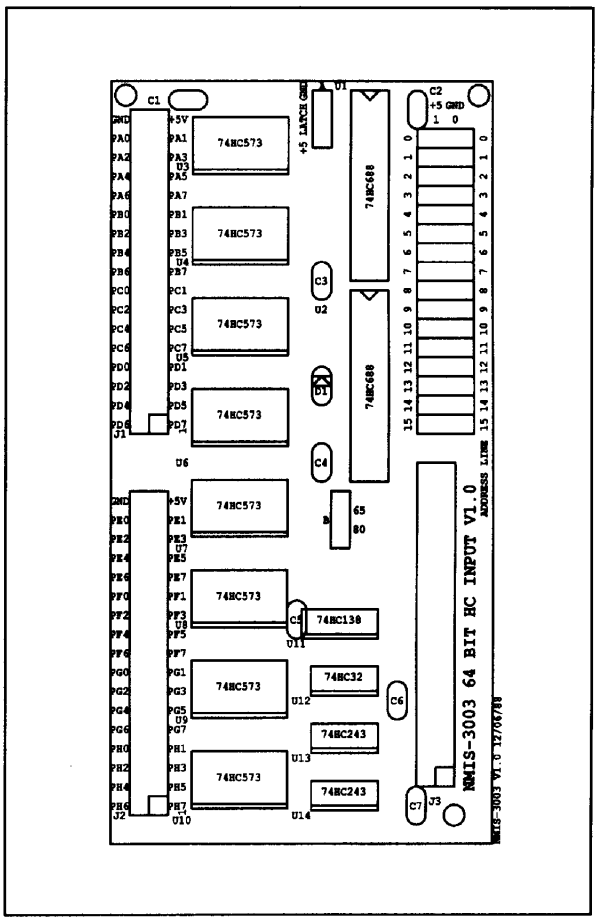
FEATURES

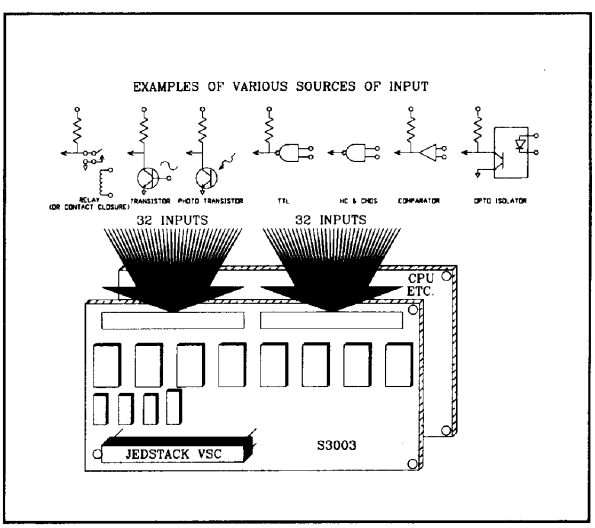
- Eight 8-bit parallel input ports
- Latchable inputs
- Low power HCMOS design
- Compact size
- Easy connection
- Easy computer interfacing

All the pins of the 34-pin connectors, J1 and J2, can attach to individual input points, except for Pin 33, which is attached to +5V power; and Pin 34, which is connected to system ground. The eight 8-bit latches are used as input gates, with optional externally-controlled latching. Two 4-bit, bidirectional transceivers buffer the data bus from the loads of the eight latches. Control logic is used to generate the chip select and timing information to operate the latches and drivers.

The latches can operate in two different ways by jumper setting. In one method, the latches are transparent, passing the input pins' current state directly to the processor. In another, the latches are transparent, until a control signal goes low. Then the readings are latched at their state at the time. The readings will continue to be read in that state, despite any changes on the external input pins, until the control signal returns high again.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the input chip's space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-3003 occupies 8 addresses. Any 8-byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.





Application

NMIS-3003

DESCRIPTION

The NMIS-3003 64-Bit Input Card is designed to stack on the 2x4"s™ NMIS Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The JEDSTACK™ provides interface signals to the board including address lines, data lines, control lines and 5V power and ground. The fast HC devices allow access times approaching 90nS.

The addressing of the octal latches on the NMIS-3003 is sensed by two 74HC688 (U1 and U2) octal comparators that decode the 13 address lines (A15 - A4) and one control line in order to select only eight active locations out of a 64K address space.

The 74HC138 uses this signal for its negative enables and the output of Jumper "B" for its one positive enable. Jumper "B" will either provide a constant high if set for "80" type processors, or the "E" clock if set for 6500 and 6800 type processors. The "E" clock is necessary for correct timing information when using a 6500 or 6800 type processor on the JEDSTACK™ bus. If the processor is a 6500 or 6800 type (such as the F68HC11), the jumper should be in the "65" position. If the processor type is an 8031 or Z80 type (such as the 8052AH), the jumper should be in the "80" position.

The address inputs to the 74HC138 include three address lines (A0, A1 and A2) and the R/W line. The eight decoded chip selects go to the 74HC573 input latches.

The 74HC573's are connected to the Data Bus by way of the 74HC243's. The 74HC243's act as bus buffers, limiting the load placed on the Data Bus to only one HC load (rather than eight). This increases the number of boards that can otherwise be put on the system, due to fan out limitations. By way of these bus drivers, the 74HC573's send data to the processor.

The center pin on Jumper "A" is the 74HC573's latch enable. When the line is high, the 74HC573's are transparent, passing the input pins' current state directly to the processor. Jumper "A" can be removed and an external signal provided to control the latch enable. When the line is high, the 74HC573's are transparent. When the line goes low the readings are latched at their state at the time. The readings will continue to be read in that state, despite any changes on the external input pins, until the line returns high again.

ADDRESS	LATCH	BITS
XXX0	1 U3	1-8 PA0-PA7
XXX1	2 U4	9-16 PB0-PB7
XXX2	3 U5	17-24 PC0-PC7
XXX3	4 U6	25-32 PD0-PD7
XXX4	5 U7	33-40 PE0-PE7
XXX5	6 U8	41-48 PF0-PF7
XXX6	7 U9	49-56 PG0-PG7
XXX7	8 U10	57-64 PH0-PH7

Register Summary

NMIS-3003

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