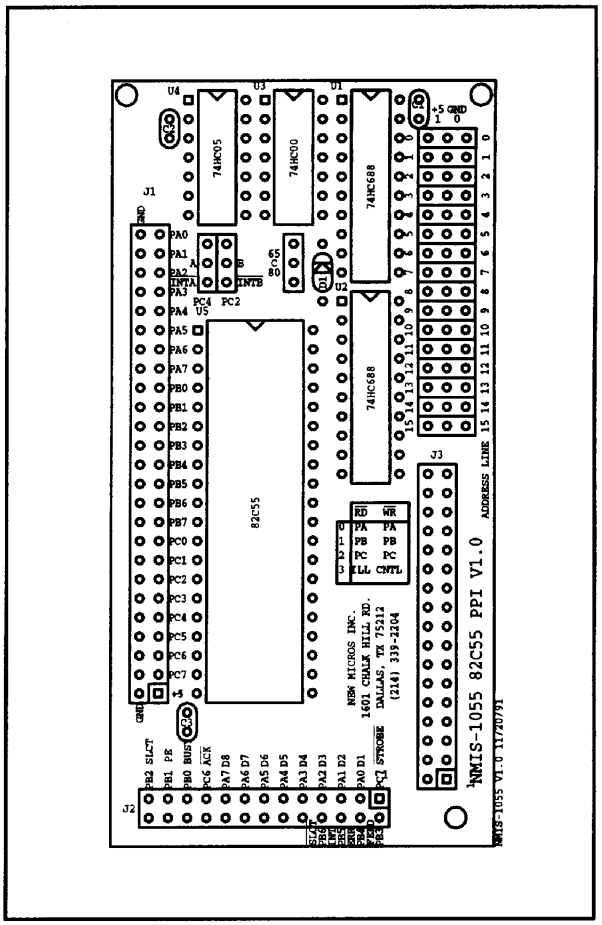
NMIS-1055 82C55 PPI BOARD

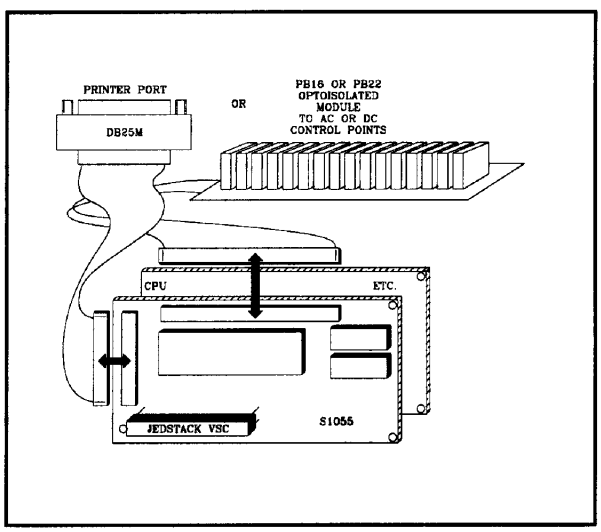
The NMIS-1055 82C55 Interface Adapter (PPI) Board provides a JEDSTACK™ computer system with 24 programmable I/O lines, or two 8-bit parallel ports with data latching and handshaking lines.



- Three 8-Bit Parallel Ports give 24 I/O pins
- Port A or B programmable as all input or output
- Port C programmable as I/O or handshake/edge-sensitive lines for Ports A and B
- Three basic operating modes
- Extended handshake capability allowing positive control of data transfers between processor and peripheral devices
- Connection for DB25 to PC compatible printer
- Connection for PB24, or individual I/O points
- Jumpers for interrupt control
- Jumper for Intel or Motorola type processor bus

The Intel 82C55 Programmable Peripheral Interface chip is mapped into the processor's address or I/O space by the card. The 82C55 controls three ports, Ports A, B and C, consisting of 24 I/O lines. The 82C55 has three operating modes. These are Basic I/O, Strobe Handshacking, or Strobed Bidirectional Bus I/O. Port A can be programmed with either all 8 lines as inputs, or, all outputs. The same is true of Port B. The direction of Port C lines are controlled by the mode. In Basic I/O, Port C acts like two 4 line ports. Either can be all 4 lines inputs, or all outputs. In the other modes, Port C lines take on input or output functions according to their handshaking function.

A Vertical Stacking Connector (VSC) in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the Programmable Peripheral Interface chip's space in memory is accomplished by two octal comparators and 16 two-position jumpers. The NMIS-1055 occupies 4 addresses. Any 4 byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.



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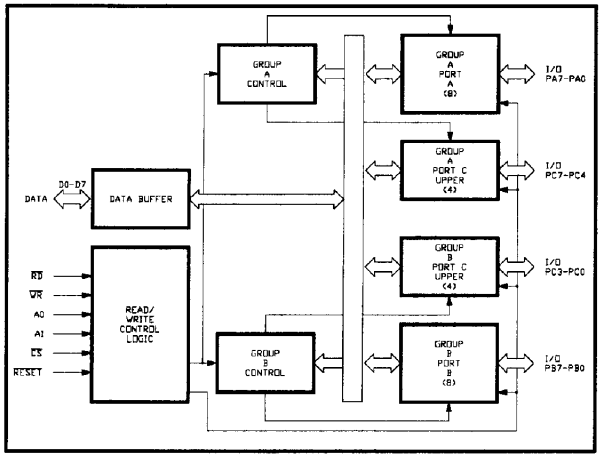
Two connectors are placed on the left and bottom edges of the board. They are labeled J1 and J2 respectively. Both connectors bring the ports of the 82C55 out for connection, each with a slightly different configuration, intended for a specific purpose. The 50-pin J1 connector offers the same signals in a pinout tailored to the industry standard PB16 and PB24 Solid State Relay boards. The 26-pin J2 connector has the PA0-PA7, PB0-PB6, PC6-7 and GND. These signals are arranged in such a fashion as to directly accommodate a parallel printer interface. A 26-pin ribbon cable from the J2 connector run to a DB25F has the same pinout as does an IBM PC printer port. A simple driver can direct output from the card to any compatible printer.



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Operation of the 82C55 is controlled by an internal, write-only Control Register. It controls the modes selected. Each port has a read-write data register.

ADDRESS	REG #	REGISTER / DESCRIPTION	
		WRITE	READ
0		Port A	
1		Port B	
2		Port C	
3		N.A.	CNTL

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In some modes, the two Port C lines associated with interrupts can serve as normal port pins. To allow dual functionality, jumpers are provided for these outputs. The jumpers feed open collector buffers hooked directly to the interrupt INT' line on the VSC. The open collector output allows other sources to share the interrupt line.

A jumper is also provided to select between processor type. The interface circuitry allows this board will work on both Motorola style (6800 and 6500) processors, as well as Intel style processors (8051, 8086, etc.). The jumper determines if timing for data transfer is taken from the E clock or the WR' and OE' signals themselves.

The NMIS-1055 PPI card is designed to stack on the 2x4"s™ NMIS Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The JEDSTACK™ provides the interface signals to the board including address lines, data lines, control lines and 5V power and ground. The 82C55 allows 150nS read and 100nS write access times.

NMIS-1055

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