

# NMIS-1022 R65C22 VIA BOARD

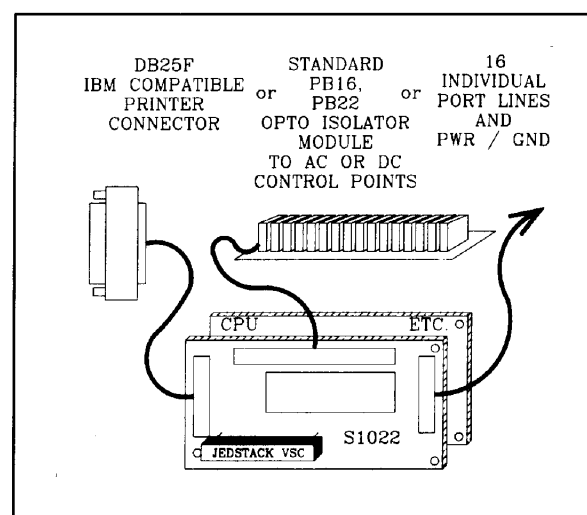
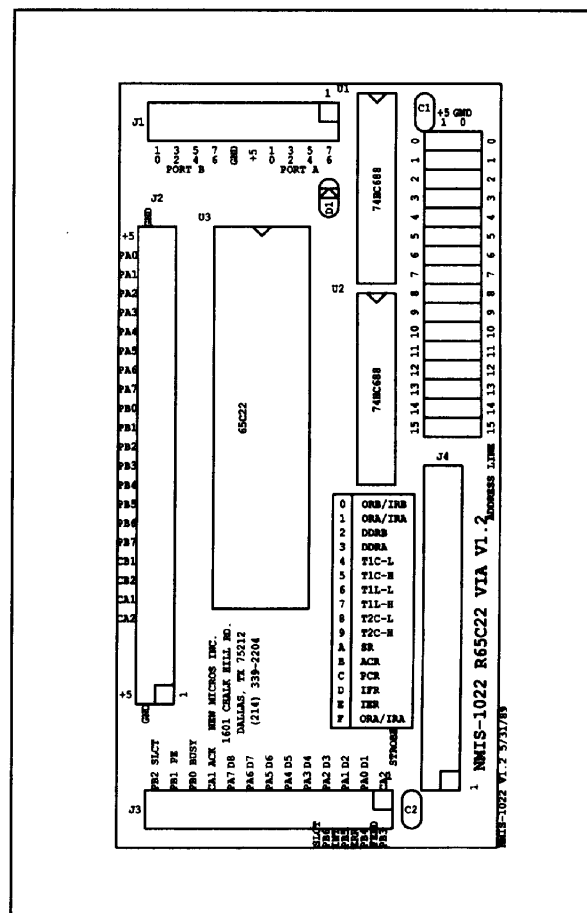
The NMIS-1022 R65C22 Versatile Interface Adapter (VIA) Board provides a JEDSTACK™ computer system with two 8-bit parallel ports, a pair of powerful 16-bit interval timers, a serial-to-parallel/parallel-to-serial shift register, data latching, and handshaking capabilities.

## FEATURES

- Two 8-Bit Parallel Ports
- Two programmable handshake/edge-sensitive lines per port
- Extended handshake capability allowing positive control of data transfers between processor and peripheral devices
- Two 16-Bit multiple mode Timer/Counters
- Synchronous Serial Channel
- Ports' connections configurable to: Printer, or PB16, or individual HCTTL level I/O Points

The Rockwell 65C22 Versatile Interface Adapter Chip is memory mapped by the card. The 65C22 includes functions for programmed control of up to two peripheral devices (Ports A and B). These two program-controlled, 8-bit, bi-directional, peripheral I/O ports allow direct interfacing between the microprocessor and the selected peripheral units. Each port has input data latching capability. Two programmable Data Direction Registers (A and B) allow selection of data direction (input or output) on an individual line basis. The R65C22 also has two programmable, 16-bit, Interval Timer/Counters with latches. Timer 1 may be operated in a One-Shot Interrupt Mode, with interrupts on each count-to-zero, or in a Free-Run Mode, with a continuous series of evenly spaced interrupts. Timer 2 functions as both an interval and pulse counter. Serial data transfers are provided by a serial-to-parallel/parallel-to-serial shift register.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the Versatile Interface Adapter chip's space in memory is accomplished by two octal comparators and 16 two-position jumpers. The NMIS-1022 occupies 16 addresses. Any 16 byte boundary in the 64K address space of the JEDSTACK™ processor's bus can be selected by correct jumper placement.



## Application

## DESCRIPTION

Three connectors line the front left and back edges of the board. They are labeled J1, J2 and J3 respectively. All three of the connectors bring the ports of the R65C22 out for connection, each with a slightly different configuration, intended for a specific purpose. The 20-pin J1 connector offers Port A, Port B, +5V and GND in the familiar pinout as the port lines of the NMIX series boards. The 50-pin J2 connector offers the same signals in a pinout tailored to the industry standard PB16 Solid State Relay boards. Additionally, the handshake control lines, CB1, CB2, CA1 and CA2, are added to spare pins in such a way that a PB24 module could control these lines. The edge-sensitive input features of these pins can be exploited in this way, although they do not make good general purpose I/O pins. The 26-pin J3 connector has the PA0-PA7, PB0-PB6, CA1-2 and GND. These signals are arranged in such a fashion as to directly accommodate a parallel printer interface. A 26-pin ribbon cable from the J2 connector run to a DB25F has the same pinout as does an IBM PC printer port. A simple driver can direct output from the card to any compatible printer.

The IRQ' output is hooked directly to the interrupt INT line on the VSC. The chip can provide interrupts to the processor with this signal. It is an "open collector" output that pulls down the pull-up on the processor board.

The NMIS-1022 VIA card is designed to stack on the 2x4's™ NMIS Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single

board computers. Because of the interface signals, how-

ADDRESS	REG #	REGISTER / DESCRIPTION	
		WRITE	READ
0	ORB / IRB	Output Register B	Input Register B
1	ORA / IRA	Output Register A	Input Register A
2	DDRB	Data Direction Register B	
3	DDRA	Data Direction Register A	
4	T1C-L	T1 Low-Order Latches	T1 Low-Order Counter
5	T1C-H	T1 High-Order Counter	
6	T1L-L	T1 Low-Order Latches	
7	T1L-H	T1 High-Order Latches	
8	T2C-L	T2 Low-Order Latches	T2 Low-Order Counter
9	T2C-H	T2 High-Order Counter	
A	SR	Shift Register	
B	ACR	Auxiliary Control Register	
C	PCR	Peripheral Control Register	
D	IFR	Interrupt Flag Register	
E	IER	Interrupt Enable Register	
F	ORA / IRA	Output Register A*	Input Register A*

Note: \*Same as Register 1 except no handshake.

## Register Summary

ever, (specifically, E clock) used by the 65C22, this

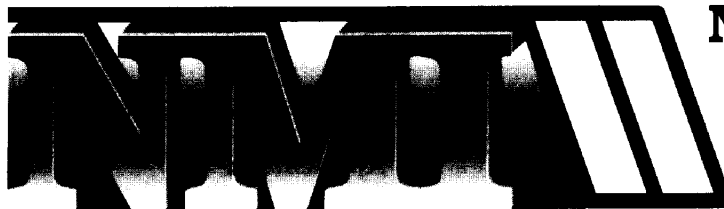
board will only work on 6800 and 6500 type processors. The JEDSTACK™ provides the interface signals to the board including address lines, data lines, control lines and 5V power and ground. The 2 MHz 65C22 allows 250nS access times.

The NMIS-1022 is designed for the Rockwell R65C22 Versatile Interface Adapter. However, there are other pin-compatible chips that are available and will work in the board. A high-operating-power NMOS version, the R6522A, is available from Rockwell. Other sources for the part include Synertek's SY6522 (now out of business) and MOS Technologies' (Commodore) MOS6522.

## WORLD HEADQUARTERS

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