

NMIS-0001 PROTOTYPING CARD

The NMIS-0001 Prototyping Card, in 2x4" sTM format provides a system designer with access to the JEDSTACKTM computer system's bus and a 1.0" by 3.8" prototype area with tenth-inch-centered .060" square pads, drilled at .036" and plated through.

FEATURES

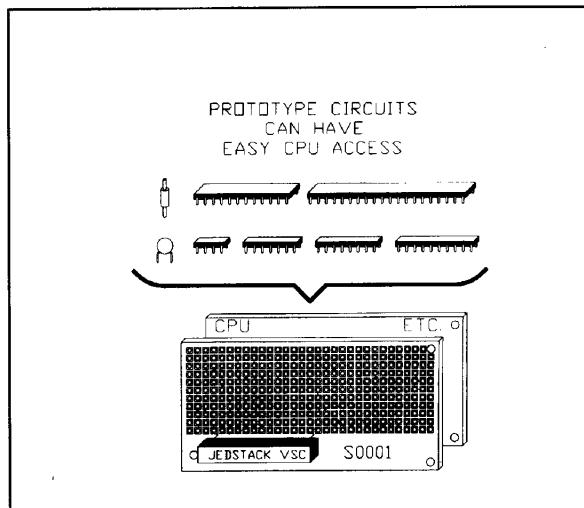
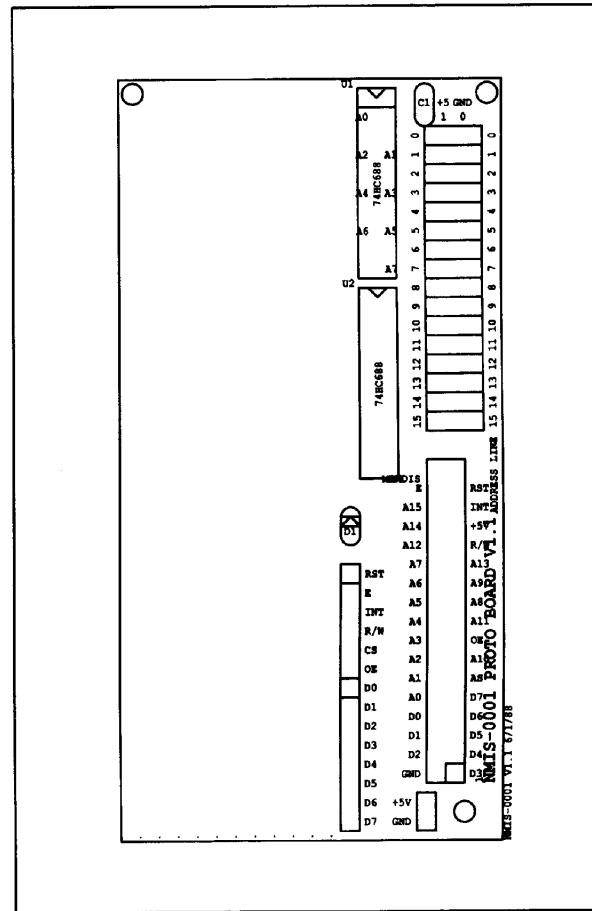
- 1.0" by 3.8" prototype area
- Tenth-inch-centered hole pattern
- Two-sided, .060" square pads
- Plated through .036" holes
- Connections provided for Data Bus (D0-D7), Output Enable (OE), decoded chip select (CS), Read/Write (R/W), interrupt (INT), E clock and Reset (RST) lines

Beyond the edge of the prototyping area, connections are provided to allow easy access to the Data Bus (D0-D7), Output Enable (OE), decoded chip select (CS), Read/Write (R/W), interrupt (INT), E clock and Reset (RST) lines.

A Vertical Stacking Connector in the lower right hand corner (top view) provides connections to the processor's address and data bus, control signals, 5V power and ground. Address decoding of the Prototyping Card's space in memory is accomplished by two octal comparators and 16 two-position jumpers. Each jumper setting corresponds to the state of a particular address line. The NMIS-0001 occupies 1 address in memory, although it can be modified to notch out 2, 4, 8, etc., up to 256 locations. Any even byte boundary, for the size of the notch addressed in the 64K address space of the JEDSTACK™ processor's bus, can be selected by correct jumper placement.

DESCRIPTION

The NMIS-0001 Prototyping Card is designed to stack on the 2x4" sTM NMIS Series, the "100 Squared"™ NMIX and the "Generic Target Computer"™ NMIT Series (with the Vertical Stacking Connector added to the latter) of single board computers. The JEDSTACK™ provides the interface signals to the board including address lines, data lines, Control lines and 5V power and ground.



Application

NMIS-0001

PROTOTYPING CARD

2x4's

The addressing of the CS output on the NMIS-0001 is created by two octal comparators that decode the 16 address lines (A15-A0) and one control line to select only one (or optionally more) active locations out of a 64K address space.

CHANGING ADDRESS WINDOW

The address locations, where the card is active, are user set by the arrangement of addressing jumpers. Each address line can be sensed for high or low condition. The user has the option of removing some address lines from the selection process. If no modifications are made to the board, the chip select generated is active for one and only one byte in the entire memory map. To select an address window of 2, 4, 8, 16, 32, 64 or 128 bytes, traces must be cut and jumpers added. Selecting a 256 byte address window does not require any cutting, and the addition of only one jumper. The user may wish to choose this method, even if the chip or chips being added require fewer locations, and allow them to "mirror map", just because of the relative ease of modification.

To modify the NMIS-0001 to "look" at only the upper eight address lines and ignore the lower eight address lines, giving a 256 location chip select, perform the following: 1) remove U1 2) install a jumper between the two holes, found on the bottom of the board underneath U1, located between Pins 1 and 20. In effect this routes the AS signal (coming from the VSC to Pin 1 of the first

74HC688) into the input of the second 74HC688 (which was previously fed by Pin 19 of U1, the output of the first 74HC688). If the address selected before modification was 8000 hex (or any address from 8000 to 80FF), the new chip select window will include the entire 8000 page (i.e., active at any address from 8000 to 80FF).

Finer resolution requires more detailed modification. To select an address window of 2, 4, 8, 16, 32, 64 or 128 bytes, U1 must be installed. The individual address lines going to U1 must be removed from their comparator input pins, and jumpers installed from those pins to the individually matching comparator input pins.

For instance, if a 2 byte address window is desired for the chip select signal, Address Line 0 must be cut from Pin 2, and Pin 2 must be jumpered to Pin 3.

The following is a table of the various address lines going to U1 by pin assignment, listed with their matching comparator inputs.

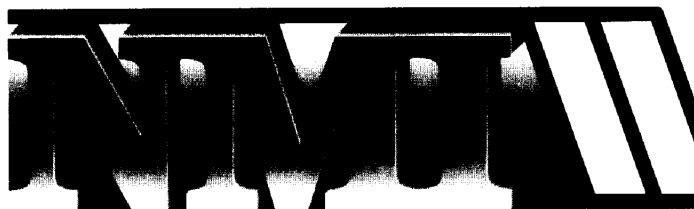
ADDRESS LINE	INPUT PIN	MATCHING INPUT	WINDOW SIZE
A0	2	3	2
A1	17	18	4
A2	4	5	8
A3	15	16	16
A4	6	7	32
A5	13	14	64
A6	8	9	128
A7	11	12	256

U1 Pin Selection

WORLD HEADQUARTERS

WORLDWIDE REPRESENTATIVES

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