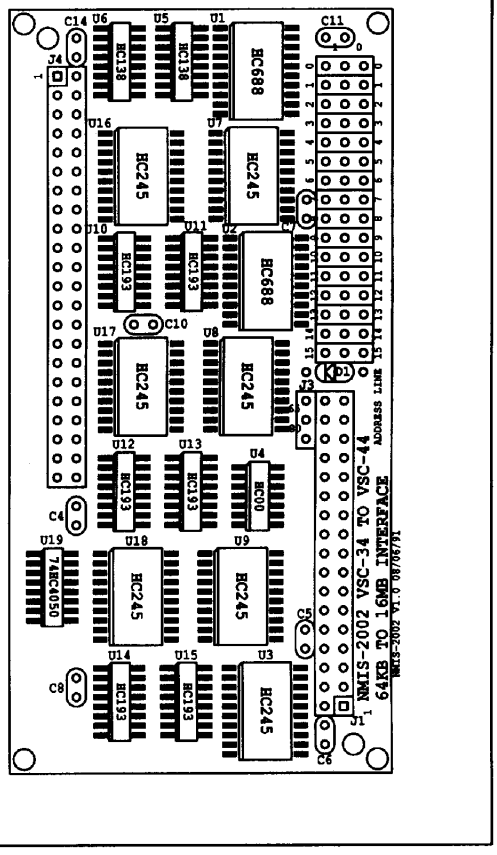
NMIS-2002 MEMORY EXPANDER CARD

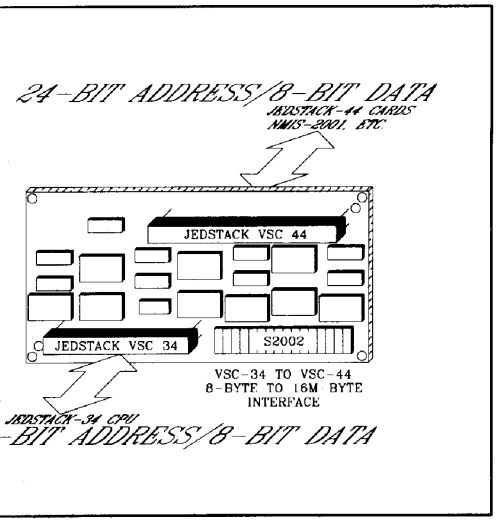
The NMIS-2002 Memory Expander Card, in 2x4"s™ format, provides a JEDSTACK-34™ computer system with a "bridge" to access JEDSTACK-44™ cards. The typical JEDSTACK-34™ processor, normally limited to 64K bytes of memory, can thereby access up to 16 Megabytes with ease. Special features facilitate sequential accessing of data in the Expanded Memory space.

FEATURES

- Expands 64K byte JEDSTACK-34™ computer system to access 16M byte JEDSTACK-44™
- Only 8 locations used in JEDSTACK-34™ map
- Creates 24 address lines via 24-bit counter/latch
- Easy check of next-address-to-be-accessed by read-back on counter/latch
- Random Access by direct-loading counter/latch
- Ascending Sequential Access by auto-post-increment of counter/latch after each byte transfer
- Descending Sequential Access by auto-post-decrement of counter/latch after each byte transfer
- Multiple NMIS-2002 can be used on one JEDSTACK-34™ computer system, each with 16M byte address space
- Multiple NMIS-2002 can be used in combination on one JEDSTACK-44™ card stack to give independent pointers for DMA-like operations

A Vertical Stacking Connector (VSC-34) in the lower right hand corner (top view) provides connections to the JEDSTACK-34™ processor's address and data bus, control signals, 5V power and ground. A second Vertical Stacking Connector (VSC-44) in the upper left hand corner, rotated by 180 degrees, provides all the bus signals for connection to a JEDSTACK-44™ stack; address lines, data bus, etc. A 24-bit up/down counter/latch functions as a pointer into Expanded Memory. A 24-bit counter/latch drives the 24-bit address bus of the JEDSTACK-44™. The counter can be read, written, and controlled by a processor on the "64K byte bus side", giving full access to the "16M byte bus side". The NMIS-2002's location in the 64K address space of the JEDSTACK-34™ processor's bus can be selected on any 8-byte boundary by correct jumper placement.





Application

NMIS-2002

NMIS-2002 MEMORY EXPANDER CARD 2x4"s

DESCRIPTION

The NMIS-2002 Memory Expander offers a VSC-34 to VSC-44 interface. It gives an 8-bit processor,which could access only 64K bytes of memory, an 8-byte to 16M byte interface. The NMIS-2002 appears as 8 registers in the host memory map. The 24-bit counter/latch may be directly written, and read back, by Registers 0, 1 and 2. Registers 4,5,and 6 are used for data transfers. For any given address, the upper registers will all act on the same data. However, if the data is transferred through Register 4, the counter will be post-decremented. A subsequent access will act on the next lower location in expanded memory. If through Register 6, the counter will be post-incremented. A subsequent access will act on the next higher location. Data transferred through Register 5, will not change the counter. This is useful in read/modify/write functions. Data can be read from Register 5, modified, and written to Register 6. The next read of Register 5, will be at the next higher location.

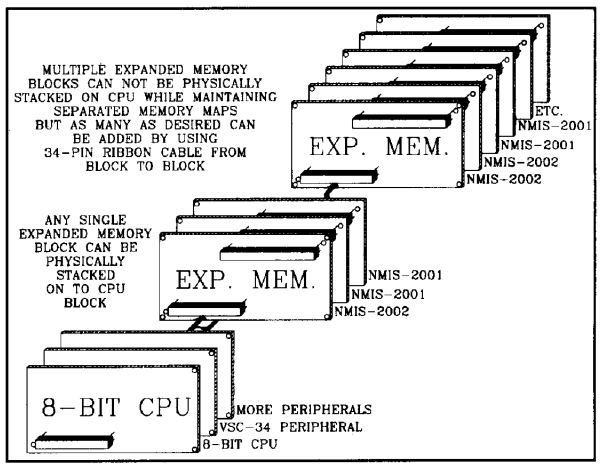
A single VSC-34 processor can have multiple NMIS-2002's. Each will have a unique 8-byte location in the processor's memory map. It is possible for each NMIS-2002's to have a separate, "private" 16M byte address space, giving even larger system memory capacities (e.g. two allows 32M bytes). Another design possibility permits several NMIS-2002's to share the same VSC-44. This allows multiple pointers in a commonly shared 16M byte space. High speed, data buffer transfers are possible if two NMIS-2002's work in the same address space. The processor need only read a byte from one, write a byte to the other, then count and loop. No intermediate reloading of the NMIS-2002's counter/latches are needed between bytes. The result can be likened to having added two 24-bit indexing registers to the CPU.

The NMIS-2002 is ideal for data logging applications. The automatic sequential data handling turns the 16M byte space into a convenient circular buffer. It excels, also, where communication needs large buffers. Using digitized audio becomes more manageable, with it, too.

NMIS-2002

ADDRESS	REGISTER
XXXX+0	HIGH BYTE COUNTER
XXXX+1	MIDDLE BYTE COUNTER
XXXX+2	LOW BYTE COUNTER
XXXX+3	RESERVED
XXXX+4	DATA, W/POST DECREMENT
XXXX+5	DATA, W/O COUNTER CHANGE
XXXX+6	DATA W/POST INCREMENT
XXXX+7	RESERVED

Register Summary



Flexible Configuration

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