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TECHNICAL DATA

19/3/98

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Technical Supplement

MC68HC912BC32 Electrical Characteristics

The MC68HC912BC32 microcontroller unit (MCU) is a16-bit device composed of standard on-chip peripherals including a 16-bit central processing unit (CPU12), 32-Kbyte flash EEPROM, 1-Kbyte RAM, 768-byte EEPROM, an asynchronous serial communications interface (SCI), a serial peripheral interface (SPI), an 8-channel timer and 16-bit pulse accumulator, a 10-bit analog-to-digital converter (ADC), a four-channel pulse-width modulator (PWM), and a CAN 2.0B compatible controller (MSCAN12). System resource mapping, clock generation, interrupt control and bus interfacing are managed by the Lite integration module (LIM). The MC68HC912BC32 has full 16-bit data paths throughout, however, the multiplexed external bus can operate in an 8-bit narrow mode so single 8-bit wide memory can be interfaced for lower cost systems.

This supplement contains the most accurate electrical information for the MC68HC912BC32 microcontroller available at the time of publication. The information should be considered preliminary and is subject to change. The following characteristics are contained in this document:

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Table 1 Maximum Ratings[1]

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}, V_{DDA}, V_{DDX}	–0.3 to +6.5	V
Input voltage	V_{IN}	–0.3 to +6.5	V
Operating temperature range[2] MC68HC912BC32FU MC68HC912BC32CFU	T_A	T_L to T_H 0 to +70 –40 to +85	°C
Storage temperature range	T_{stg}	–55 to +150	°C
Current drain per pin[3] Excluding V_{DD} and V_{SS}	I_{IN}	±25	mA
V_{DD} differential voltage	$V_{DD}–V_{DDX}$	6.5	V

NOTES:
1. Permanent damage can occur if maximum ratings are exceeded. Exposures to voltages or currents in excess of recommended values affects device reliability. Device modules may not operate normally while being exposed to electrical extremes.
2. Refer to MC68HC912BC32TS/D Technical Summary for complete part numbers.
3. One pin at a time, observing maximum power dissipation limits. Internal circuitry protects the inputs against damage caused by high static voltages or electric fields; however, normal precautions are necessary to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. Extended operation at the maximum ratings can adversely affect device reliability. Tying unused inputs to an appropriate logic voltage level (either GND or V_{DD}) enhances reliability of operation.

Table 2 Thermal Characteristics

Characteristic	Symbol	Value	Unit
Average junction temperature	T_J	$T_A + (P_D \times \Theta_{JA})$	°C
Ambient temperature	T_A	User-determined	°C
Package thermal resistance (junction-to-ambient) 80-pin quad flat pack (QFP)	Θ_{JA}	85	°C/W
Total power dissipation[1]	P_D	$P_{INT} + P_{I/O}$ or $\frac{K}{T_J + 273°C}$	W
Device internal power dissipation	P_{INT}	$I_{DD} \times V_{DD}$	W
I/O pin power dissipation[2]	$P_{I/O}$	User-determined	W
A constant[3]	K	$P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2$	W · °C

NOTES:
1. This is an approximate value, neglecting $P_{I/O}$.
2. For most applications $P_{I/O} \ll P_{INT}$ and can be neglected.
3. K is a constant pertaining to the device. Solve for K with a known T_A and a measured P_D (at equilibrium). Use this value of K to solve for P_D and T_J iteratively for any value of T_A.

Table 3 DC Electrical Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Input high voltage, all inputs	V_{IH}	$0.7 \times V_{DD}$	$V_{DD} + 0.3$	V
Input low voltage, all inputs	V_{IL}	V_{SS}–0.3	$0.2 \times V_{DD}$	V
Output high voltage, all I/O and output pins except XTAL Normal drive strength I_{OH} = –10.0 µA I_{OH} = –0.8 mA Reduced drive strength I_{OH} = –4.0 µA I_{OH} = –0.3 mA	V_{OH}	 $V_{DD} - 0.2$ $V_{DD} - 0.8$ $V_{DD} - 0.2$ $V_{DD} - 0.8$	 — — — —	 V V V V
Output low voltage, all I/O and output pins except XTAL Normal drive strength I_{OL} = 10.0 µA I_{OL} = 1.6 mA Reduced drive strength I_{OL} = 3.6 µA I_{OL} = 0.6 mA	V_{OL}	 — — — —	 V_{SS}+0.2 V_{SS}+0.4 V_{SS}+0.2 V_{SS}+0.4	 V V V V
Input leakage current[1] $V_{in} = V_{DD}$ or V_{SS} All input only pins except $\overline{IRQ}$, ATD[2] and V_{FP} $V_{in} = V_{DD}$ or V_{SS} $\overline{IRQ}$	I_{in}	 — —	 ±2.5 ±10	 µA µA
Three-state leakage, I/O ports, BKGD, and $\overline{RESET}$	I_{OZ}	—	±2.5	µA
Input capacitance All input pins and ATD pins (non-sampling) ATD pins (sampling) All I/O pins	C_{in}	 — — —	 10 15 20	 pF pF pF
Output load capacitance All outputs except PS[7:4] PS[7:4] when configured as SPI	C_L	 — —	 90 200	 pF pF
Programmable active pull-up current $\overline{XIRQ}$, $\overline{DBE}$, $\overline{LSTRB}$, R/$\overline{W}$, ports A, B, DLC, P, S, T MODA, MODB active pull down during reset BKGD passive pull up	I_{APU}	 50 50 50	 500 500 500	 µA µA µA

NOTES:
1. Specification is for parts in the -40 to +85°C range. Higher temperature ranges will result in increased current leakage.
2. See **Table 6 ATD DC Electrical Characteristics**.

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Table 4 Supply Current

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	8 MHz Typical	2 MHz	4 MHz	8 MHz	Unit
Maximum total supply current						
RUN:	I_{DD}					
Single-chip mode			15	25	45	mA
Expanded mode			25	45	70	mA
WAIT: (All peripheral functions shut down)	W_{IDD}					
Single-chip mode			1.5	3	5	mA
Expanded mode			4	7	10	mA
STOP:	S_{IDD}					
Single-chip mode, no clocks –40 to +85			10	10	10	µA
Maximum power dissipation[1]	P_D					
Single-chip mode			75	125	225	mW
Expanded mode			125	225	350	mW

NOTES:
1. Includes I_{DD} and I_{DDA}.

Table 5 ATD Maximum Ratings

Characteristic	Symbol	Value	Units
ATD reference voltage			
$V_{RH} \le V_{DDA}$	V_{RH}	–0.3 to +6.5	V
$V_{RL} \ge V_{SSA}$	V_{RL}	–0.3 to +6.5	V
V_{SS} differential voltage	$\lvert V_{SS}–V_{SSA} \rvert$	0.1	V
V_{DD} differential voltage	$V_{DD}–V_{DDA}$	6.5	V
	$V_{DDA}–V_{DD}$	0.3	V
V_{REF} differential voltage	$\lvert V_{RH}–V_{RL} \rvert$	6.5	V
Reference to supply differential voltage	$\lvert V_{RH}–V_{DDA} \rvert$	6.5	V

Table 6 ATD DC Electrical Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
Analog supply voltage	V_{DDA}	4.5	5.5	V
Analog supply current, normal operation	I_{DDA}		1.0	mA
Reference voltage, low	V_{RL}	V_{SSA}	$V_{DDA}/2$	V
Reference voltage, high	V_{RH}	$V_{DDA}/2$	V_{DDA}	V
V_{REF} differential reference voltage[1]	$V_{RH}–V_{RL}$	4.5	5.5	V
Input voltage[2]	V_{INDC}	V_{SSA}	V_{DDA}	V
Input current, off channel[3]	I_{OFF}		100	nA
Reference supply current	I_{REF}		250	µA
Input capacitance Not Sampling Sampling	C_{INN} C_{INS}		10 15	pF pF

NOTES:

1. Accuracy is guaranteed at $V_{RH} - V_{RL}$ = 5.0V ±10%.
2. To obtain full-scale, full-range results, $V_{SSA} \leq V_{RL} \leq V_{INDC} \leq V_{RH} \leq V_{DDA}$.
3. Maximum leakage occurs at maximum operating temperature. Current decreases by approximately one-half for each 10°C decrease from maximum temperature.

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Table 7 Analog Converter Characteristics (Operating)

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Typical	Max	Unit
8-Bit resolution[1]	1 count		20		mV
8-Bit Differential non-linearity[2]	DNL	–0.5		+0.5	count
8-Bit Integral non-linearity[2]	INL	–1		+1	count
8- Bit Absolute error[2,3]	AE	–1		+1	count
10-Bit Resolution[1]	1 count		5		mV
10-Bit Differential non-linearity[2]	DNL	-1		1	count
10-Bit Integral non-linearity[2]	INL	-2		2	count
10-Bit Absolute error[2, 3]	AE	-2.5		2.5	count
Maximum source impedance	R_S		20	See note[4]	KΩ

NOTES:

1. $V_{RH} – V_{RL} \geq 5.12V$; $V_{DDA} – V_{SSA} = 5.12V$
2. At V_{REF} = 5.12V, one 8-bit count = 20 mV, and one 10-bit count = 5mV.
3. These values include quantization error which is inherently 1/2 count for any A/D converter.
4. Maximum source impedance is application-dependent. Error resulting from pin leakage depends on junction leakage into the pin and on leakage due to charge-sharing with internal capacitance.
   Error from junction leakage is a function of external source impedance and input leakage current. Expected error in result value due to junction leakage is expressed in voltage (V_{ERRJ}):

$$V_{ERRJ} = R_S \times I_{OFF}$$

where I_{OFF} is a function of operating temperature. Charge-sharing effects with internal capacitors are a function of ATD clock speed, the number of channels being scanned, and source impedance. For 8-bit conversions, charge pump leakage is computed as follows:

$$V_{ERRJ} = .25pF \times V_{DDA} \times R_S \times ATDCLK/(8 \times \text{number of channels})$$

Table 8 ATD AC Characteristics (Operating)

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, ATD Clock = 2 MHz, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
MCU clock frequency (p-clock)	f_{PCLK}	2.0	8.0	MHz
ATD operating clock frequency	f_{ATDCLK}	0.5	2.0	MHz
ATD 8-Bit conversion period clock cycles[1] conversion time[2]	n_{CONV8} t_{CONV8}	18 9	32 16	cycles µs
ATD 10-Bit conversion period clock cycles[1] conversion time[2]	n_{CONV10} t_{CONV10}	20 10	34 17	cycles µs
Stop and ATD power up recovery time[3] VDDA = 5.0V	t_{SR}		10	µs

NOTES:
1. The minimum time assumes a final sample period of 2 ATD clock cycles while the maximum time assumes a final sample period of 16ATD clocks.
2. This assumes an ATD clock frequency of 2.0MHz.
3. From the time ADPU is asserted until the time an ATD conversion can begin.

Table 9 EEPROM Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Typical	Max	Unit
Minimum programming clock frequency[1]	f_{PROG}	1.0			MHz
Programming time	t_{PROG}			10	ms
Clock recovery time, following STOP, to continue programming	t_{CRSTOP}			t_{PROG}+ 1	ms
Erase time	t_{ERASE}			10	ms
Write/erase endurance		10,000	30,000[2]		cycles
Data retention		10			years

NOTES:
1. RC oscillator must be enabled if programming is desired and $f_{SYS} < f_{PROG}$.
2. If average T_H is below 85° C.

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Table 10 Flash EEPROM Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Typical	Max	Units
Program/erase supply voltage: Read only Program / erase / verify[1]	V_{FP}	 V_{DD}–0.35 11.0	 V_{DD} 11.4	 V_{DD}+0.5 11.8	 V V
Program/erase supply current Word program(V_{FP} = 12V) Erase(V_{FP} = 12V)	I_{FP}			 30 4	 mA mA
Number of programming pulses	n_{PP}			50	pulses
Programming pulse	t_{PPULSE}	20		25	µs
Program to verify time	t_{VPROG}	10			µs
Program margin	p_m	100[2]			%
Number of erase pulses	n_{EP}			5	pulses
Erase pulse	t_{EPULSE}	90	100	110	ms
Erase to verify time	t_{VERASE}	1			ms
Erase margin	e_m	100[2]			%
Program/erase endurance		100			cycles
Data retention		10			years

NOTES:
1. Refer to errata for problem description and suggested workaround.
2. The number of margin pulses required is the same as the number of pulses used to program or erase.

Table 11 Pulse Width Modulator Characteristics

V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Characteristic	Symbol	Min	Max	Unit
E-clock frequency	f_{eclk}		8.0	MHz
A-clock frequency Selectable	f_{aclk}	f_{eclk}/128	f_{eclk}	Hz
B-clock frequency Selectable	f_{bclk}	f_{eclk}/128	f_{eclk}	Hz
Left-aligned PWM frequency 8-bit 16-bit	f_{lpwm}	 f_{eclk}/1M f_{eclk}/256M	 f_{eclk}/2 f_{eclk}/2	 Hz Hz
Left-aligned PWM resolution	r_{lpwm}	f_{eclk}/4K	f_{eclk}	Hz
Center-aligned PWM frequency 8-bit 16-bit	f_{cpwm}	 f_{eclk}/2M f_{eclk}/512M	 f_{eclk} f_{eclk}	 Hz Hz
Center-aligned PWM resolution	r_{cpwm}	f_{eclk}/4K	f_{eclk}	Hz

Table 12 Control Timing

Characteristic		Symbol	8.0 MHz		Unit
			Min	Max	
Frequency of operation		f_o	dc	8.0	MHz
E-clock period		t_{cyc}	125	—	ns
Crystal frequency		f_{XTAL}	—	16.0	MHz
External oscillator frequency		$2f_o$	dc	16.0	MHz
Processor control setup time	$t_{PCSU} = t_{cyc}/2 + 20$	t_{PCSU}	82	—	ns
Reset input pulse width To guarantee external reset vector Minimum input time (can be preempted by internal reset)		PW_{RSTL}	32 2	— —	t_{cyc} t_{cyc}
Mode programming setup time		t_{MPS}	4	—	t_{cyc}
Mode programming hold time		t_{MPH}	10	—	ns
Interrupt pulse width, $\overline{IRQ}$ edge-sensitive mode	$PW_{IRQ} = 2t_{cyc} + 20$	PW_{IRQ}	270	—	ns
Wait recovery startup time	$t_{WRS} = 4t_{cyc}$	t_{WRS}	—	TBD	t_{cyc}
Timer input capture pulse width	$PW_{TIM} = 2t_{cyc} + 20$	PW_{TIM}	270	—	ns
Pulse accumulator pulse width		PW_{PA}	TBD	—	ns

NOTES:

1. $\overline{RESET}$ is recognized during the first clock cycle it is held low. Internal circuitry then drives the pin low for 16 clock cycles, releases the pin, and samples the pin level 8 cycles later to determine the source of the interrupt.

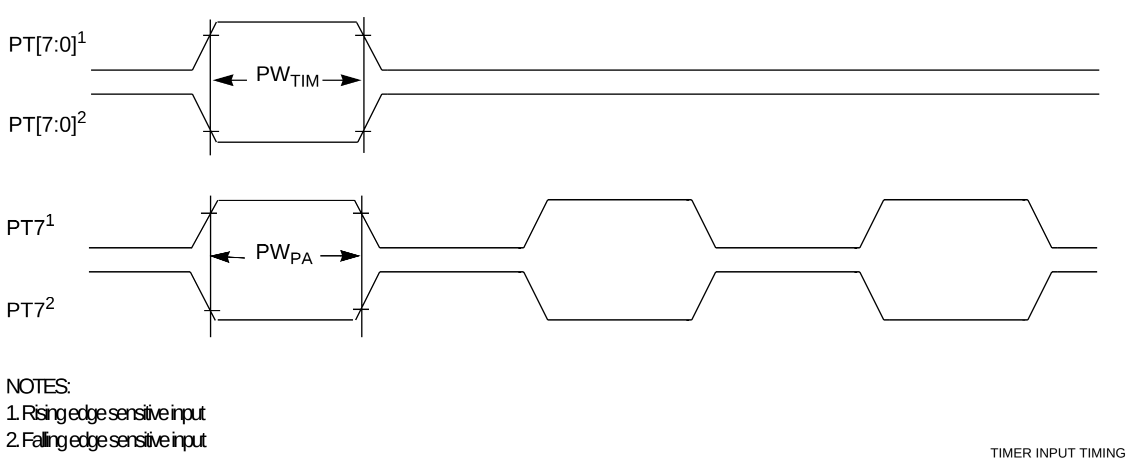
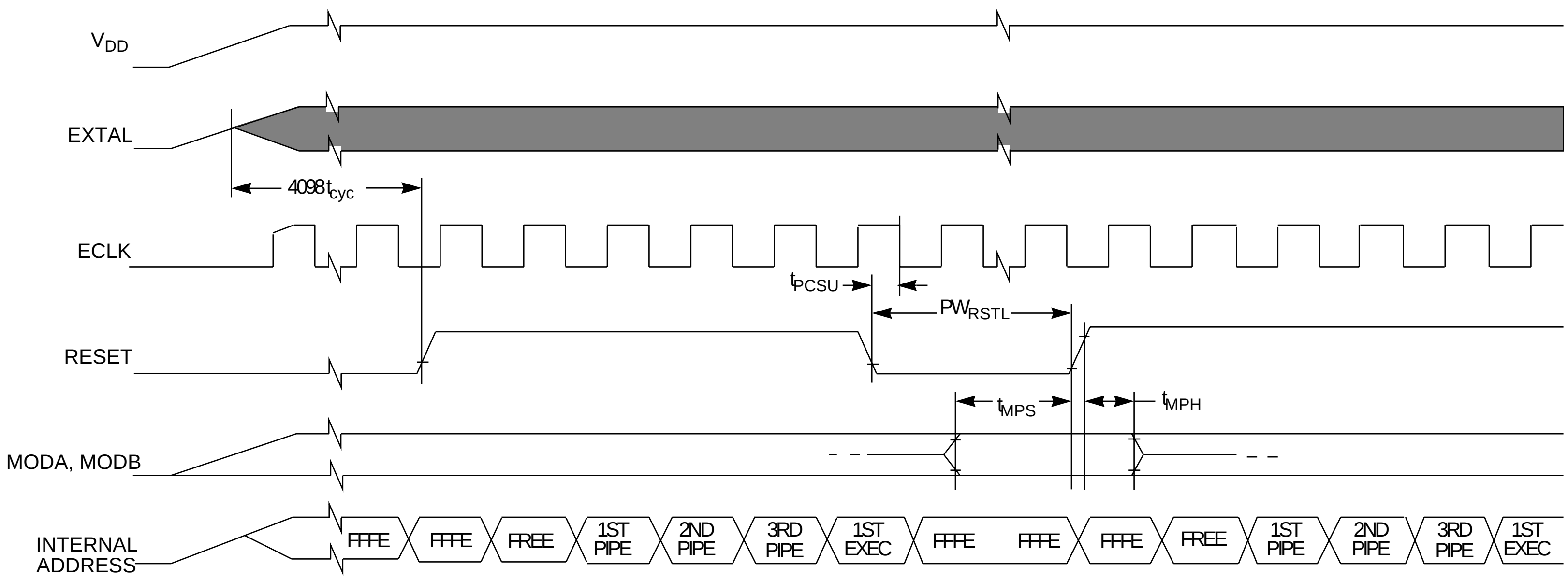


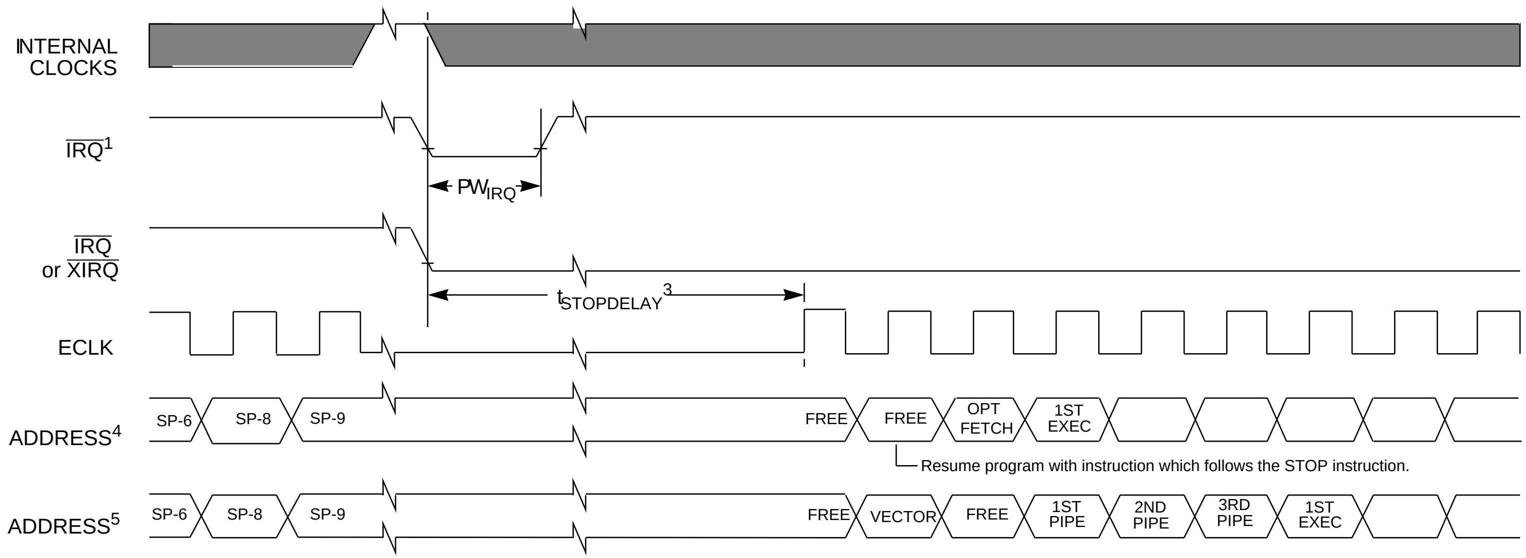
Figure 1 Timer Inputs

PRELIMINARY

Figure 2 POR and External Reset Timing Diagram



NOTE: Reset timing is subject to change.



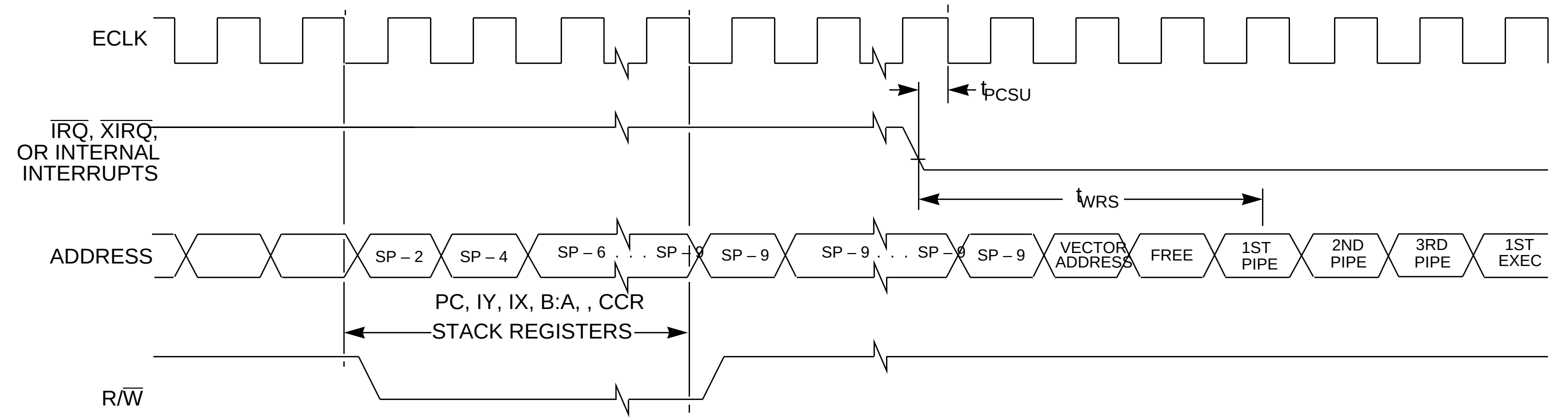
NOTES:
1. Edge Sensitive $\overline{IRQ}$ pin (IRQE bit = 1)
2. Level sensitive $\overline{IRQ}$ pin (IRQE bit = 0)
3. $t_{STOPDELAY}$ = 4098 t_{cyc} if DLY bit = 1 or 2 t_{cyc} if DLY = 0.
4. $\overline{XIRQ}$ with X bit in CCR = 1.
5. $\overline{IRQ}$ or ($\overline{XIRQ}$ with X bit in CCR = 0).

STOP RECOVERY TIM

Figure 3 STOP Recovery Timing Diagram

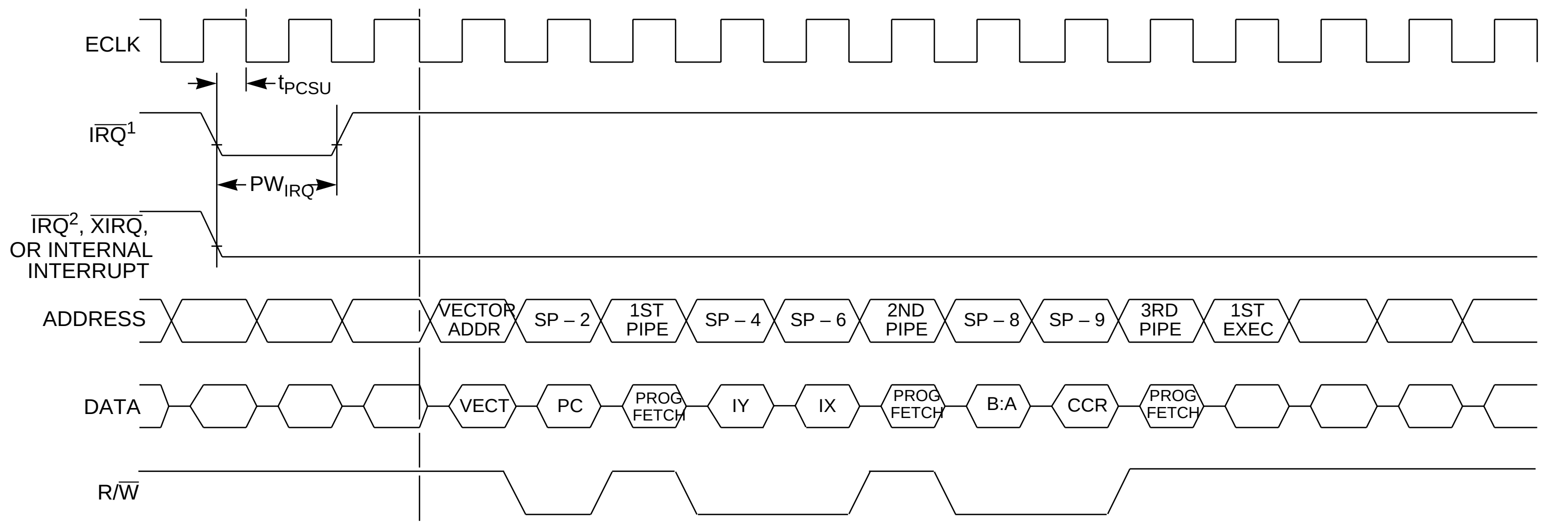
PRELIMINARY

PRELIMINARY



NOTE: RESET also causes recovery from WAIT.

Figure 4 WAIT Recovery Timing Diagram



NOTES:
1. Edge sensitive IRQ pin (IRQE bit = 1)
2. Level sensitive IRQ pin (IRQE bit = 0)

INTERRUPT TIM

Figure 5 Interrupt Timing Diagram

PRELIMINARY

Table 13 Peripheral Port Timing

Characteristic	Symbol	8.0 MHz		Unit
		Min	Max	
Frequency of operation (E-clock frequency)	f_o	dc	8.0	MHz
E-clock period	t_{cyc}	125	—	ns
Peripheral data setup time MCU read of ports $t_{PDSU} = t_{cyc}/2 + 40$	t_{PDSU}	102	—	ns
Peripheral data hold time MCU read of ports	t_{PDH}	0	—	ns
Delay time, peripheral data write MCU write to ports except Port CAN	t_{PWD}	—	40	ns
Delay time, peripheral data write MCU write to Port CAN	t_{PWD}	—	71	ns

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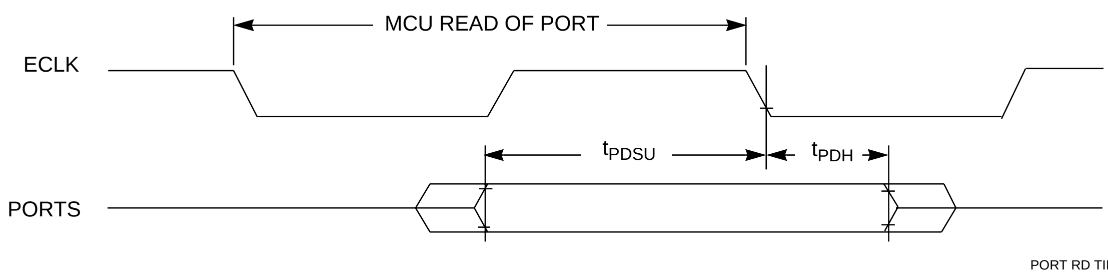


Figure 6 Port Read Timing Diagram

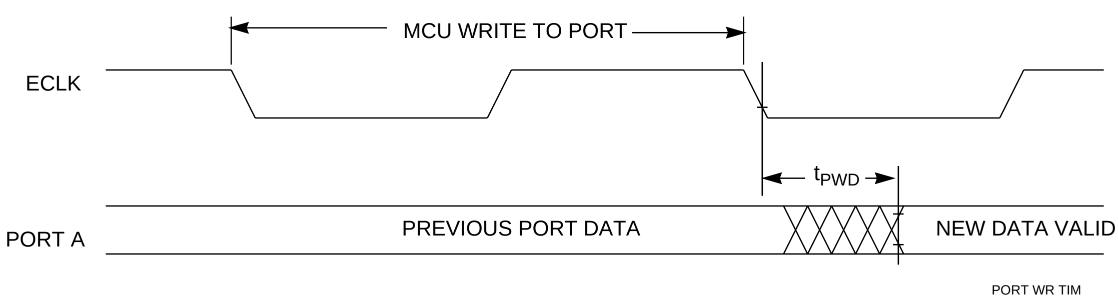


Figure 7 Port Write Timing Diagram

Table 14 Multiplexed Expansion Bus Timing

V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted

Num	Characteristic[1, 2, 3, 4]	Delay	Symbol	8 MHz		Unit
				Min	Max	
	Frequency of operation (E-clock frequency)		f_o	dc	8.0	MHz
1	Cycle time $t_{cyc} = 1/f_o$	—	t_{cyc}	125	—	ns
2	Pulse width, E low $PW_{EL} = t_{cyc}/2 + delay$	–2	PW_{EL}	60	—	ns
3	Pulse width, E high[5] $PW_{EH} = t_{cyc}/2 + delay$	–2	PW_{EH}	60	—	ns
5	Address delay time $t_{AD} = t_{cyc}/4 + delay$	29	t_{AD}	—	60	ns
7	Address valid time to ECLK rise $t_{AV} = PW_{EL} - t_{AD}$	—	t_{AV}	0	—	ns
8	Multiplexed address hold time $t_{MAH} = t_{cyc}/4 + delay$	–21	t_{MAH}	10	—	ns
9	Address Hold to Data Valid	—	t_{AHDS}	30	—	
10	Data Hold to High Z $t_{DHZ} = t_{AD} - 20$	—	t_{DHZ}	—	20	
11	Read data setup time	—	t_{DSR}	30	—	ns
12	Read data hold time	—	t_{DHR}	0	—	ns
13	Write data delay time	—	t_{DDW}	—	47	ns
14	Write data hold time	—	t_{DHW}	20	—	ns
15	Write data setup time[5] $t_{DSW} = PW_{EH} - t_{DDW}$	—	t_{DSW}	15	—	ns
16	Read/write delay time $t_{RWD} = t_{cyc}/4 + delay$	18	t_{RWD}	—	49	ns
17	Read/write valid time to E rise $t_{RWV} = PW_{EL} - t_{RWD}$	—	t_{RWV}	20	—	ns
18	Read/write hold time	—	t_{RWH}	20	—	ns
19	Low strobe[6] delay time $t_{LSD} = t_{cyc}/4 + delay$	18	t_{LSD}	—	49	ns
20	Low strobe[6] valid time to E rise $t_{LSV} = PW_{EL} - t_{LSD}$	—	t_{LSV}	11	—	ns
21	Low strobe[6] hold time	—	t_{LSH}	20	—	ns
22	Address access time[5] $t_{ACCA} = t_{cyc} - t_{AD} - t_{DSR}$	—	t_{ACCA}	—	35	ns
23	Access time from E rise[5] $t_{ACCE} = PW_{EH} - t_{DSR}$	—	t_{ACCE}	—	30	ns
24	$\overline{DBE}$ delay from ECLK rise[5] $t_{DBED} = t_{cyc}/4 + delay$	6	t_{DBED}	—	37	ns
25	$\overline{DBE}$ valid time $t_{DBE} = PW_{EH} - t_{DBED}$	—	t_{DBE}	23	—	ns
26	$\overline{DBE}$ hold time from ECLK fall	—	t_{DBEH}	0	10	ns

NOTES:
1. All timings are calculated for normal port drives.
2. Crystal input is required to be within 45% to 55% duty.
3. Reduced drive must be off to meet these timings.
4. Unequalled loading of pins will affect relative timing numbers.
5. This characteristic is affected by clock stretch.
   Add $N \times t_{cyc}$ where N = 0, 1, 2, or 3, depending on the number of clock stretches.
6. Without TAG enabled.

PRELIMINARY

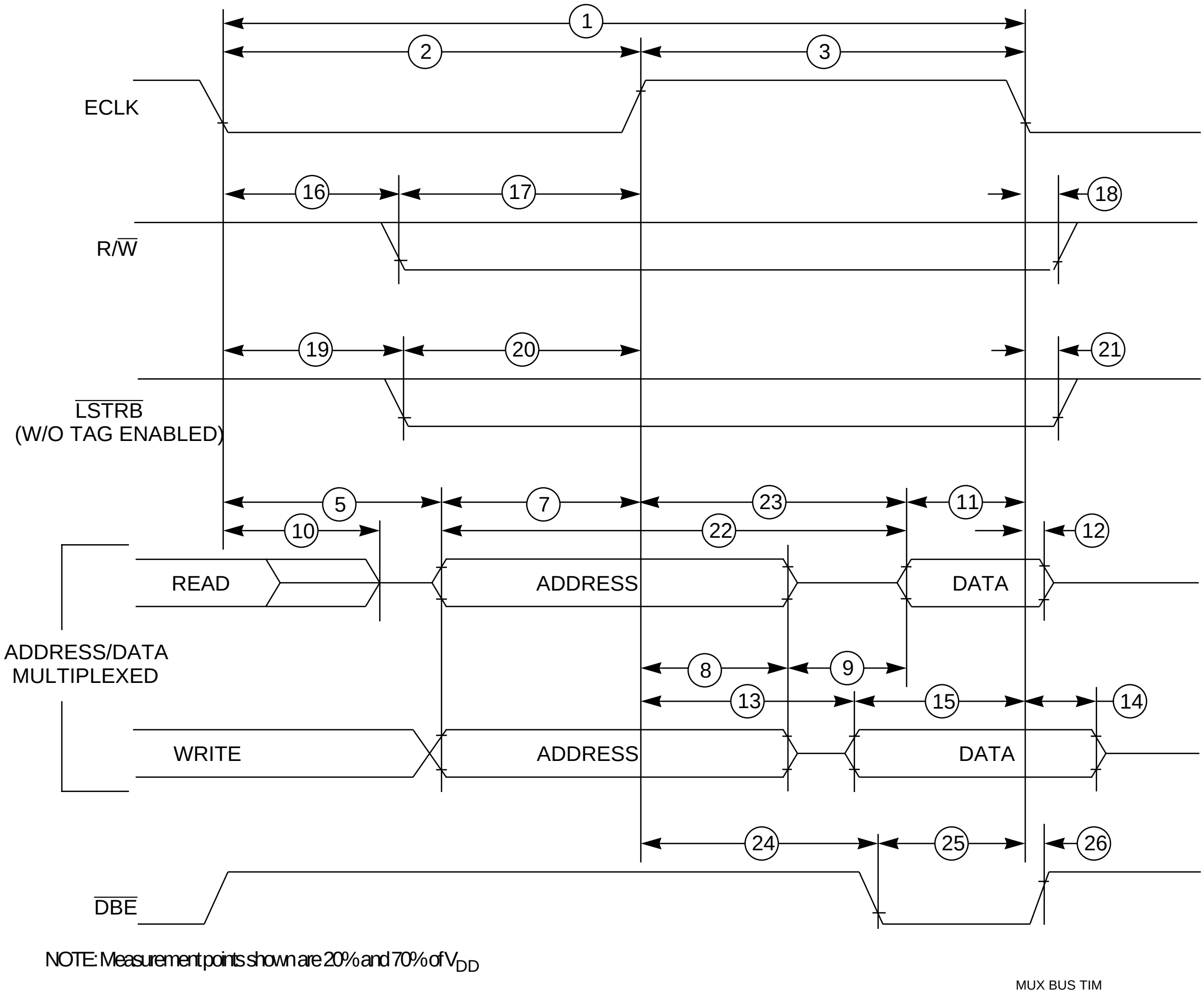


Figure 8 Multiplexed Expansion Bus Timing Diagram

PRELIMINARY

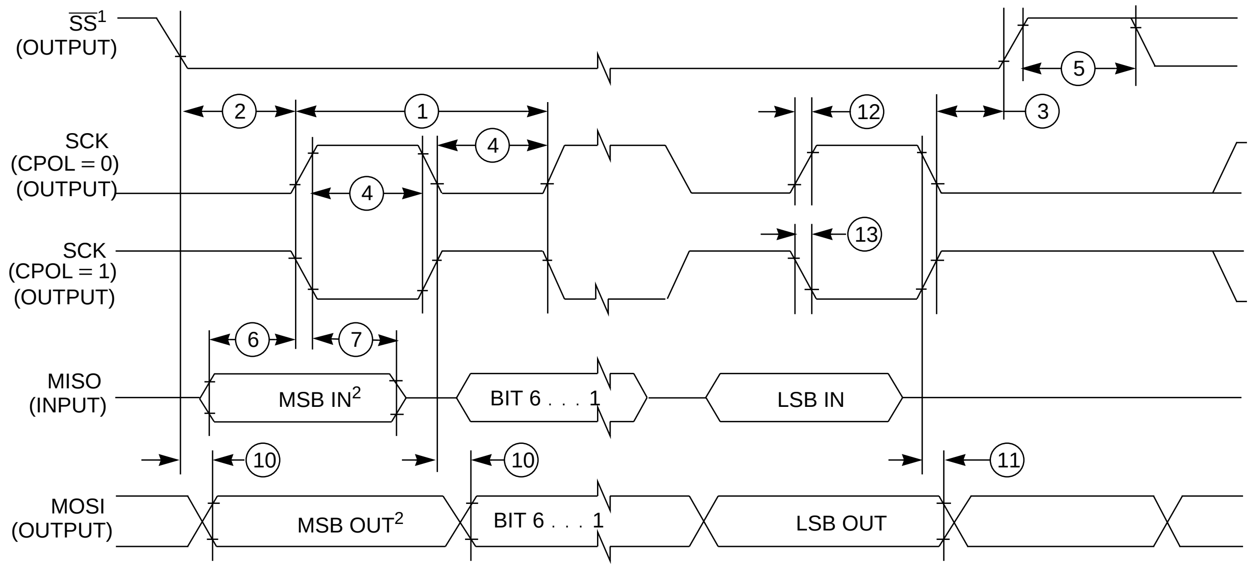
Table 15 SPI Timing

(V_{DD} = 5.0 Vdc ±10%, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H , 200 pF load on all SPI pins)[1]

Num	Function	Symbol	Min	Max	Unit
	Operating Frequency Master Slave	f_{op}	 DC DC	 1/2 1/2	E-clock frequency
1	SCK Period Master Slave	t_{sck}	 2 2	 256 —	 t_{cyc} t_{cyc}
2	Enable Lead Time Master Slave	t_{lead}	 1/2 1	 — —	 t_{sck} t_{cyc}
3	Enable Lag Time Master Slave	t_{lag}	 1/2 1	 — —	 t_{sck} t_{cyc}
4	Clock (SCK) High or Low Time Master Slave	t_{wsck}	 t_{cyc} – 60 t_{cyc} – 30	 128 t_{cyc} —	 ns ns
5	Sequential Transfer Delay Master Slave	t_{td}	 1/2 1	 — —	 t_{sck} t_{cyc}
6	Data Setup Time (Inputs) Master Slave	t_{su}	 30 30	 — —	 ns ns
7	Data Hold Time (Inputs) Master Slave	t_{hi}	 0 30	 — —	 ns ns
8	Slave Access Time	t_a	—	1	t_{cyc}
9	Slave MISO Disable Time	t_{dis}	—	1	t_{cyc}
10	Data Valid (after SCK Edge) Master Slave	t_v	 — —	 50 50	 ns ns
11	Data Hold Time (Outputs) Master Slave	t_{ho}	 0 0	 — —	 ns ns
12	Rise Time Input Output	 t_{ri} t_{ro}	 — —	 t_{cyc} – 30 30	 ns ns
13	Fall Time Input Output	 t_{fi} t_{fo}	 — —	 t_{cyc} – 30 30	 ns ns

NOTES:
1. All AC timing is shown with respect to 20% V_{DD} and 70% V_{DD} levels unless otherwise noted.

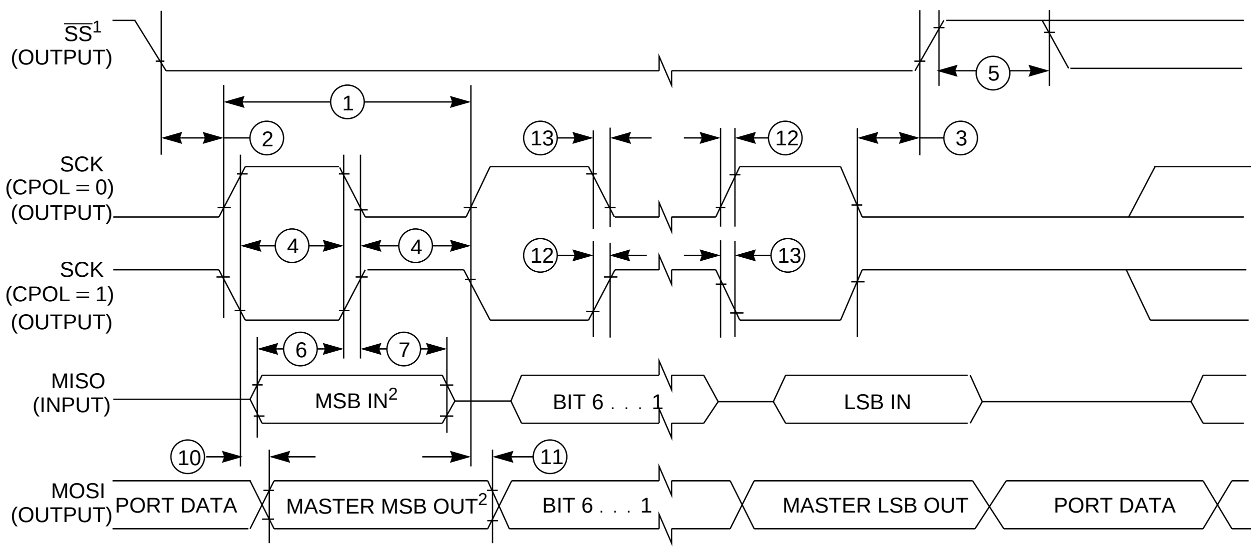
PRELIMINARY



1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

SPI MASTER CPHA0

A) SPI Master Timing (CPHA = 0)

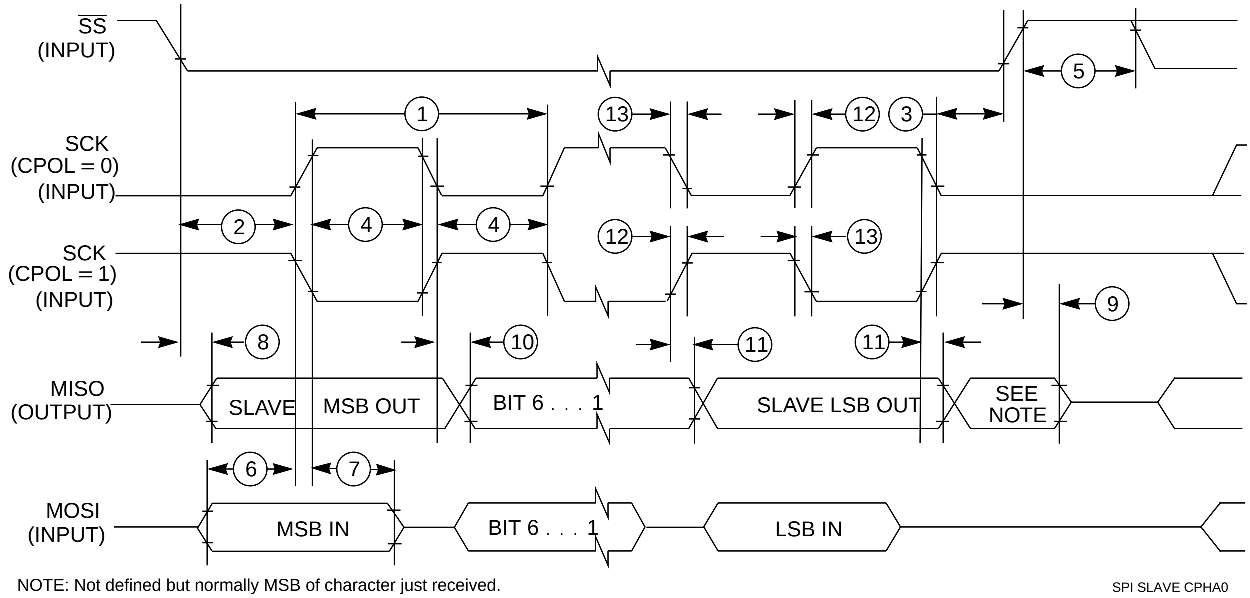


1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

SPI MASTER CPHA1

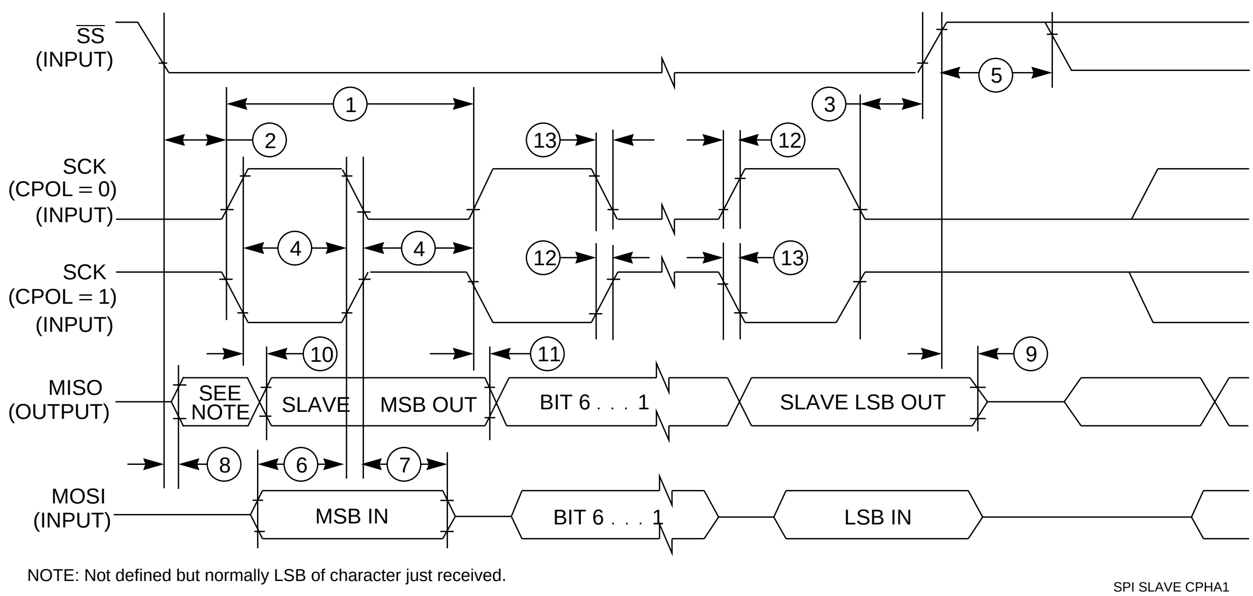
B) SPI Master Timing (CPHA = 1)

Figure 9 SPI Timing Diagram (1 of 2)



NOTE: Not defined but normally MSB of character just received.

A) SPI Slave Timing (CPHA = 0)



NOTE: Not defined but normally LSB of character just received.

B) SPI Slave Timing (CPHA = 1)

Figure 10 SPI Timing Diagram (2 of 2)

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